Carbon Nano-Relays for Low Power Switching

by

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B.S., University of California at Berkeley (2003)

Submitted to the Department of Materials Science and Engineering
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Abstract

In this thesis two unique carbon based nanoelectromechanical switches or carbon nano-relays are demonstrated as a toolkit for investigating NEMs based low power switching. The first is a vertical carbon nano-relay, consisting of a vertically aligned carbon nanotube/fiber (CN) between two contacts and operated by pull-off, and the second, a double graphene switch, consisting of two electromechanically actuated stacked layers of polycrystalline graphene.

Vertical carbon nano-relays were initially prototyped by inserting a CN between two contacts through the use of a nanopositioner. The prototype demonstrated pull-off operation and multiple switching. To our knowledge this is the only example to date of a multiple-use NEMs switch that operates with pull-off. Next a wafer integrated device was fabricated. Although pull-in was demonstrated in these integrated devices, pull-off was not possible primarily due to limitations in CN growth, which were also investigated.

In the work on a double graphene switch we demonstrated an electromechanical switch comprising two polycrystalline graphene films, each deposited using ambient pressure chemical vapor deposition (CVD). The top film is pulled into electrical contact with the bottom film by application of approximately 5V between the layers. Contact is broken by mechanical restoring forces after bias is removed. The device switches several times before tearing. Demonstration of multiple switching at low voltage confirms that graphene is an attractive material for electromechanical switches.

Thesis Supervisor: Marc A. Baldo
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Acknowledgments

As I near the end of my time as a Ph.D. student, I am happy to finally have the opportunity to thank and acknowledge all of those that I have made my Ph.D. possible be it by valuable discussions, assistance in the lab, or even with a much needed pat on the back.

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For their contributions to my work on vertical carbon nano-relays, I owe a great debt of gratitude to my collaborators Courtney Schmitt, who not only worked side-by-side me on the project for two years but was essentially in keeping me focused and organized throughout the entire process, and Luis F. Velsquez-Garca, who, despite having one of the busiest schedules I have see, still made time to help work on and discuss key aspects of the project. And of course, none of the work would have been possible without Bob Bicchieri and his constant maintenance of CCNT tool which was critical to my research on vertical carbon nano-relays.

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fabricated.

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Chapter 1

Motivation

According to the latest edition of the International Technology Roadmap for Semiconductors (ITRS), power consumption, and thus dissipation, are now the major problems facing the semiconductor industry. [1] In fact Figure 1-1 shows expected power trends from the ITRS roadmap for 2003 and 2005, indicating that after about 2005 power dissipation can no longer be increased due to limitations in system level cooling.

While a variety of techniques are available to reduce the dynamic power problem, such as device scaling, reductions in clock-speed (Figure 1-2), clock gating, dynamic voltage and frequency scaling, and better chip design used to circumvent non-essential computation, the static power dissipation, both with due to subthreshold and gate leakage have become extremely significant. Static power dissipation is still dominated by gate current leakage, but subthreshold current leakage is seen as the leading limitation since the development of high k-dielectrics as gate insulators have brought gate current leakage under control. [1]

1.1 Background

Most electronic devices today contain integrated circuits which use CMOS technology. (Figure 1-3) The power dissipated from these integrated circuits comes from two sources.

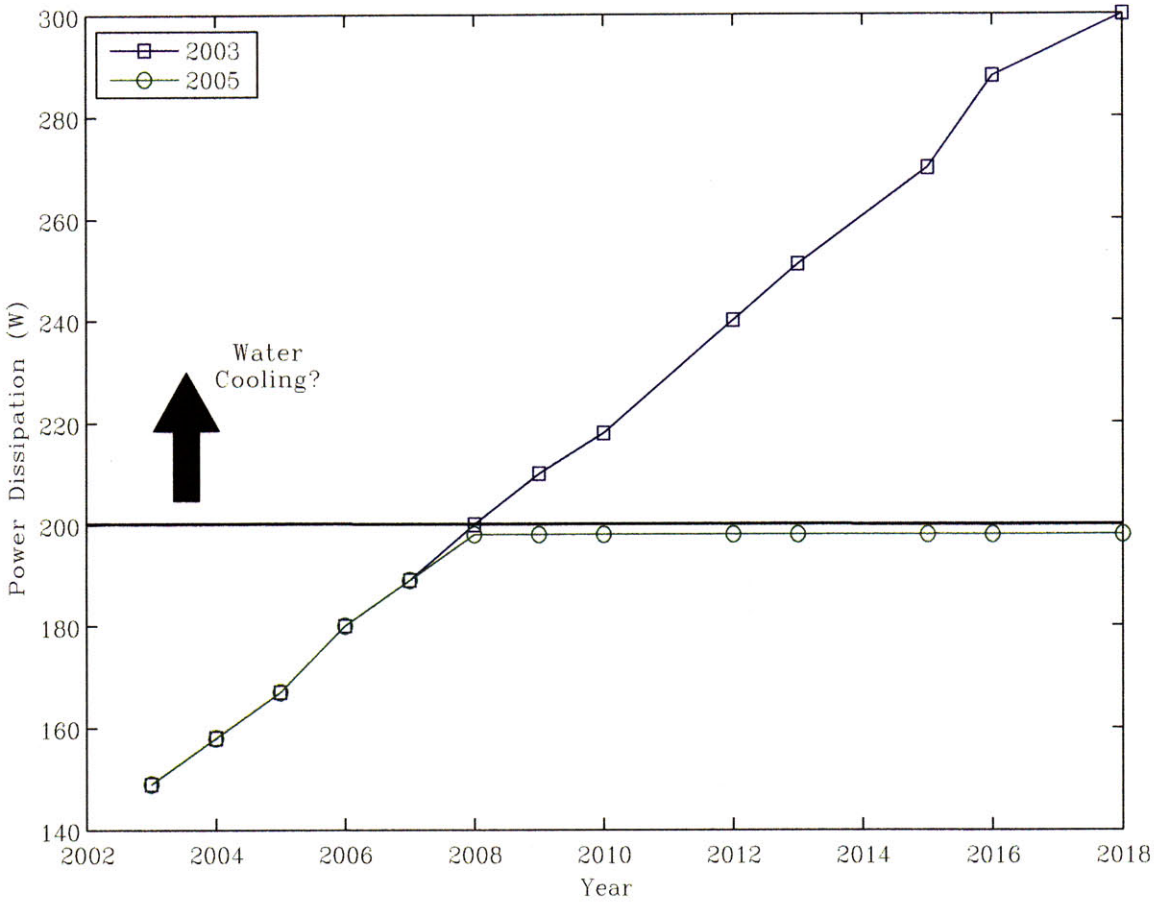


Figure 1-1: Power trend versus time. Source 2003 and 2005 International Technology Roadmap for Semiconductors update.

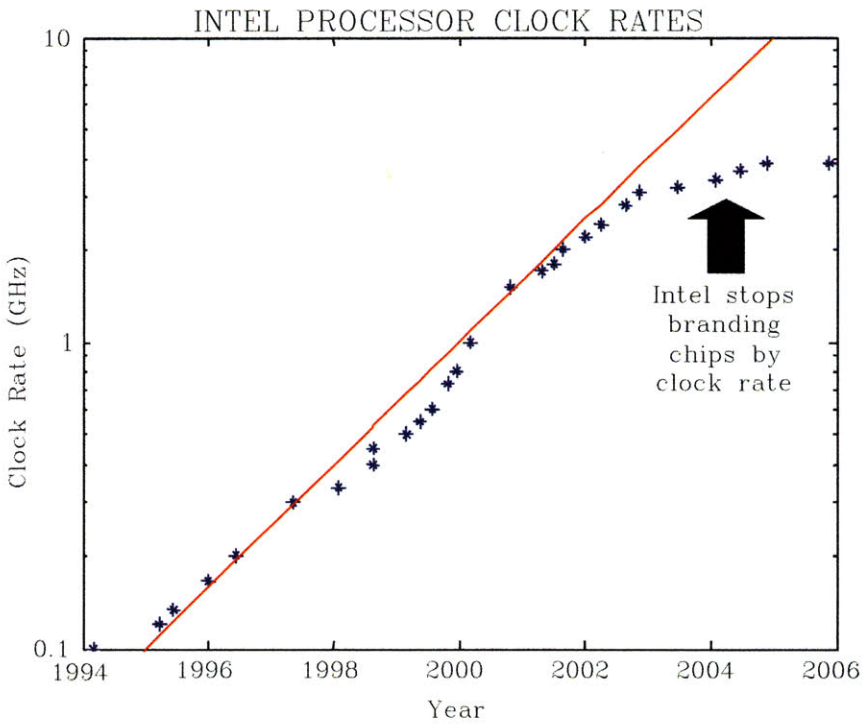


Figure 1-2: Clock rates versus time. Highlights the recent trend in reducing clock rate for dynamic power reduction.

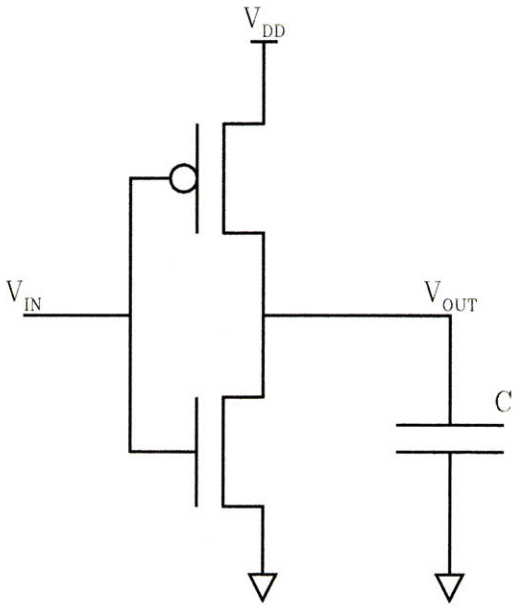


Figure 1-3: A CMOS inverter consisting of a PMOS (top) and NMOS inverter (bottom) in series. Assuming that two CMOS inverters are cascaded the second CMOS inverter is modeled by a capacitor.

$$P_{total} = P_{dyn} + P_{stat} \tag{1.1}$$

The first of which is dynamic power, i.e. power that's dissipated anytime we turn one of these CMOS switching elements on and off, and the second of which is static power, i.e. the power that's dissipated when the device is not switching. In the past dynamic power was the major contributor to the total power budget, and the solution to this problem was to scale down the device. Unfortunately, static or leakage power has increased exponentially as devices get smaller and smaller, and is now seen as the dominant contributor to power dissipation. Both sources of power dissipation will be discussed in the following sections.

1.1.1 MOSFET

CMOS technology utilizes a pair of complementary metal oxide semiconductor field effect transistors (MOSFETs), an n-type MOSFET (NMOS) and a p-type MOSFET (PMOS). A schematic of an NMOS is shown in Figure 1-4A. In an ideal MOSFET, current will only flow from the source to the drain upon electrostatic actuation of the channel via an applied gate-source bias or V_{GS} that needs to be greater than a threshold voltage V_T. For maximum gate control, it is important that the electrostatic coupling between the gate and the channel be greater than that between the source and the channel. These two electrostatic couplings can be modeled as two capacitors C_G, between the gate and the channel, and C_S, between the source and the channel, Figure 1-4B. To achieve this level of gate control it is important that $C_{GS} \gg C_{SD}$.

1.1.2 Dynamic Power

It is important to know how a CMOS circuit functions and where the source of power dissipation in the dynamic regime arises. A model CMOS circuit is shown in Figure 1-3. In CMOS circuits, ideally, power is only dissipated during switching (dynamic power) and does not dissipate power in the steady state (static power). As an example, first consider the case when V_{IN} is "low", i.e. $V_{IN} \sim 0$, and and thus for the NMOS

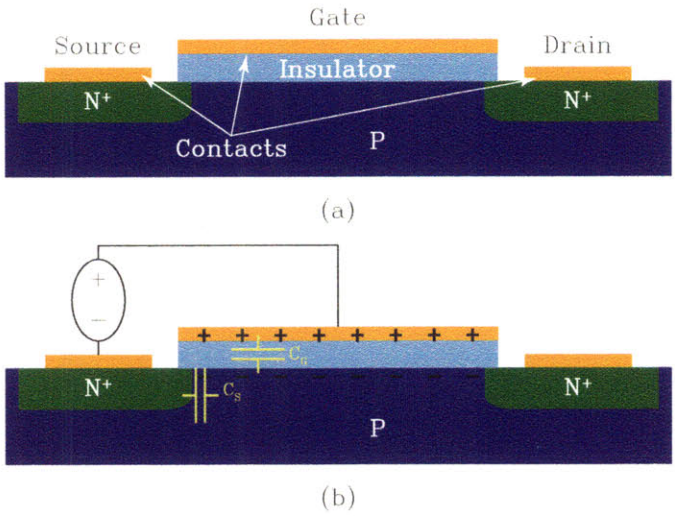


Figure 1-4: (a) A schematic of an n-type MOSFET (NMOS). (b) Electrostatic coupling in FET may be modeled by two capacitors.

$V_{GS} < V_T$ and for the PMOS $V_{GS}\,|-V_{DD}| > |V_T|$, where $|V_T|$ is the threshold voltage required to turn the NMOS or PMOS on and thus the NMOS is off and the PMOS is on. Under this condition, the capacitor C is then charged to V_{DD} and thus the output is considered "high". Considering the opposite case where the input is "high" i.e. $V_{IN} \sim V_{DD}$ for reasons previous stated the NMOS is on and the PMOS is off, the capacitor is then discharged through the NMOS FET and the output is "low". In either case, there is no current flowing directly from the power supply to ground when there is no switching. Current only flows only when the capacitor is charged or discharged. Given this basic understanding of CMOS circuitry the key characteristics of CMOS are now considered.

1.1.2.1 Power-Delay Product

As previously stated, ideally power is only dissipated when a CMOS circuit changes state, i.e. when the capacitor is being either charged or discharged. For an ideal capacitor the work done each time it is turned off and on is given by the well known formula:

$$W = \frac{1}{2}\frac{Q^2}{C}$$

Assuming the capacitor goes full cycle, from "low" to "high", from 0 to V_{DD} when charging and discharging, the capacitance is given by:

$$C = \frac{Q}{V_{DD}} \tag{1.2}$$

Thus the work done per capacitor charge/discharge cycle in a CMOS circuit, also known as the power-delay product (PDP), can be expressed as:

$$PDP = CV_{DD}^2 \tag{1.3}$$

Assuming that the switch is operated as a frequency, f, the dynamic power dissipation is:

$$P_{Dyn} = CV_{DD}^2 f \tag{1.4}$$

The PDP thus describes a fundamental trade off between power dissipation and switching speed, and it is apparent from Equation 1.4 that faster computing requires reductions in PDP.

1.1.2.2 Switching speed

The switching speed is limited by the time necessary to charge and discharge the capacitor, C. Since the current, I, can be defined in the steady state as:

$$I = \frac{Q}{t} \tag{1.5}$$

Then the maximum frequency,f_{max} is obtained by combining Equations 1.2 and 1.5 to obtain the following relation:

$$f_{\max} = \frac{I}{CV_{DD}} \tag{1.6}$$

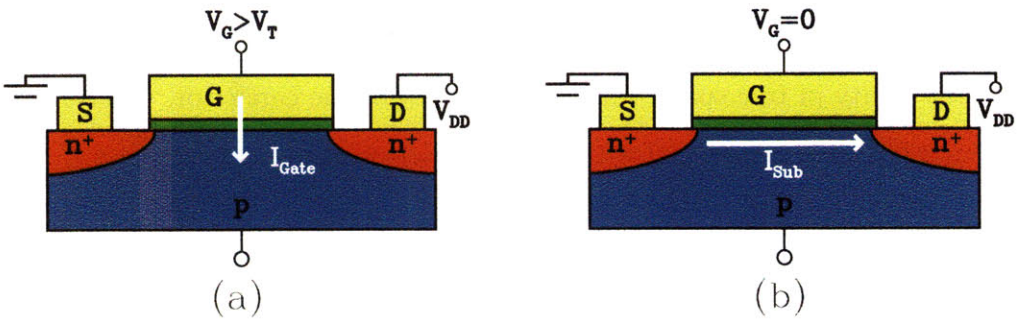


Figure 1-5: a) Gate leakage arising from current flow between the gate to the drain when the MOSFET is turned "on" and b) Subthreshold leakage arising from current flow between the source and the drain when the MOSFET is turned "off"

1.1.3 Static Power

Static power arises from power dissipation of a MOSFET during periods when switching does not occur and is thus always present. Although there are several contributors to static power dissipation the two most significant sources are gate current leakage when the MOSFET is turned "on", Figure 1-5a and subthreshold current leakage when the MOSFET is turned "off," Figure 1-5b.

1.1.3.1 Gate Leakage

The requirement from Section 1.1.1 for our MOSFET, that $C_G \gg C_S$, implies that that the $t_{ox} \ll L$. As the length scale of devices decrease so does the thickness of the oxide, eventually leading to the point where t_{ox} is thin enough that there is direct tunneling of electrons from the gate to the channel upon an applied bias, V_{GS}. This results in the gate leakage that increases exponentially as the oxide thickness is continually decreased and the contribution to the state power dissipation can be quite significant. Recent breakthroughs in high-k dielectric have brought gate leakage under control. This can be understood by considering the gate-channel capacitance to be a parallel plate capacitor, and whose capacitance can be modeled by the following equation:

$$C = \frac{k\varepsilon_0 A}{t_{ox}} \tag{1.7}$$

where k is the relative dielectric constant of the material between the plates, ε_0 is the permittivity of free space, and A is the area of the capacitor. Then relative to SiO_2 with a k=3.9, if a material with a higher dielectric constant such as HfO_2 with a k$\sim$25, and assuming that the capacitance needs to remain the same or better then the following equation can be obtained for an equivalent thickness of HfO_2:

$$t_{HfO_2} = \frac{k_{HfO_2}}{k_{SiO_2}} t_{SiO_2} \tag{1.8}$$

Since $k_{HfO_2} > 6 \times k_{SiO_2}$ the gate thickness is much greater than there is a drastic decrease in gate leakage for an equivalent capacitance. This is problem that for the most part can be overcome with selection of different materials.

1.1.3.2 Subthreshold Leakage

The second source of leakage is the subthreshold current leakage and with the breakthrough in new high-k dielectric materials discussed in the previous section is seen as the performance limiting issue in future electronics. [1] Subthreshold current leakage can be explained by examining the conduction bands of a MOSFET like an NMOS in Figure 1-6. As a note, the analysis in this section assumes that the MOSFET is ideal, meaning that, again, control of the channel is dominated by capacitance the between the gate and the channel.

In a perfect world, in the "off" state the electrons would not move between the source and drain because of the energy barrier between the source and channel, in practice this is not the case and will be discussed shortly. The way this channel switches on and off is by lowering the channel energy level, through the application of a gate-source bias, low enough such that the energy level of the channel matches that of the source and drain allowing the electrons to easily flow. The voltage necessary to achieve this condition is the threshold voltage, V_{th} and is something designers would like to drive down because of it's relation the supply voltage, V_{DD}, and in turn dynamic power.

As stated before, the "off" state is not exactly off and a certain number of elec-

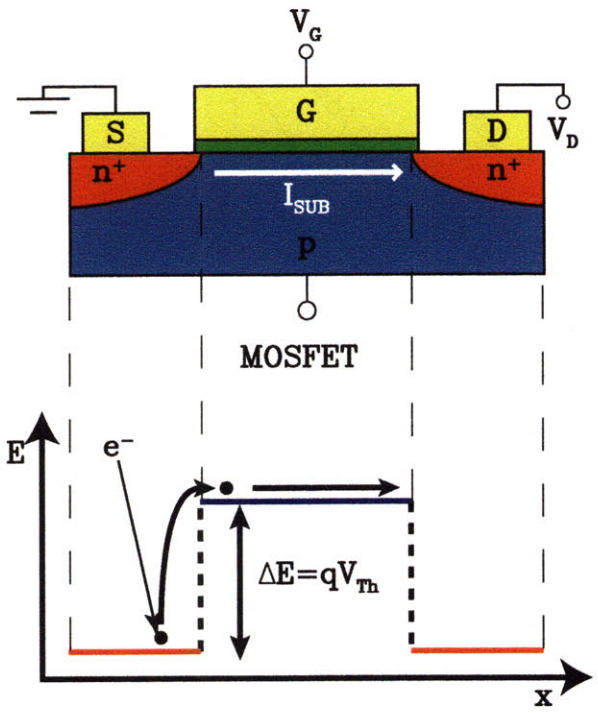


Figure 1-6: An NMOS and the corresponding conduction band energy diagram.

trons, N_e are excited above this energy barrier resulting in the subthreshold leakage. The likelihood that an electron in the source will be able to hop the barrier is given by Boltzmann statistics giving an leakage current:

$$I_{Sub} \sim N_e \sim \exp\left(-\frac{\Delta E}{kT}\right) = \exp\left(-\frac{qV_{Th}}{kT}\right) \tag{1.9}$$

This is the origin of the subthreshold leakage.

Of course, as V_{GS} increases from 0, more and more current will flow until $V_{GS} = V_{Th}$. (Figure 1-7) The slope, S, as the current is increasing in the subthreshold region is defined as:

$$\begin{aligned} S &= V_{GS}/\log_{10}(I) \\ &= -kT/q\log_{10}(I) \\ &= 60\text{mV/decade} \end{aligned} \tag{1.10}$$

The slope thus defines a fundamental limit for the subthreshold leakage in field effect transistor and as previously stated is governed by the Boltzmann statistics of

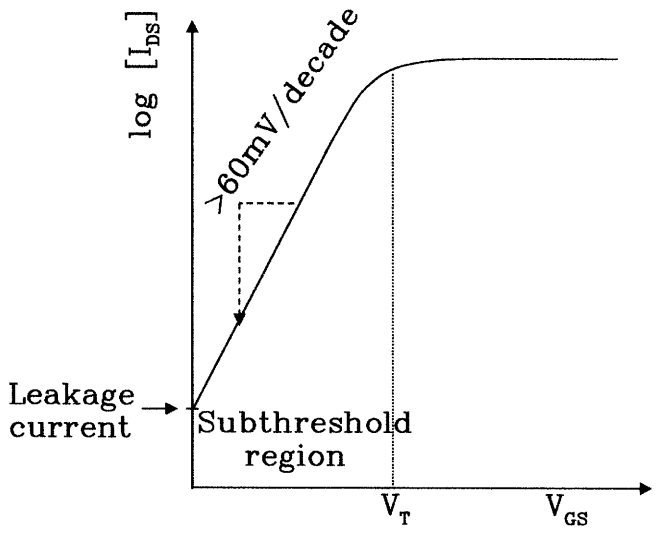


Figure 1-7: Plot of the source-drain current as a function of gate-source bias.

a single electron.

Why is this important? If the overall goal is to drive down the total power consumption, than from a dynamic power consumption stand point it is important to drive down the supply voltage and also decrease the threshold voltage. The threshold voltage is decreased by altering the energy barrier through means such as doping. From Figure 1-8, a decrease in threshold voltage results in an increase in leakage. So it is then left up to designers to come up with a balance between dynamic and static power loses. The ideal solution, seen in Figure 1-9, is to increase the subthreshold swing, or decrease the slope, and therein have the ability to decrease the threshold voltage while maintaining or potentially decreasing the subthreshold leakage through the device, and in turn decrease the power dissipation of the device as a whole. Of course, as previously discussed, the 60 mV/decade is a fundamental limit and is not a parameter that is tunable in current MOSFETs or any such electrostatically modulated devices with independent charges.

1.2 Fundamental Limits of Power Dissipation

Having set some basic limits on power dissipation by logic devices based on CMOS, is is important to set a lower bar to power dissipation by understanding what are

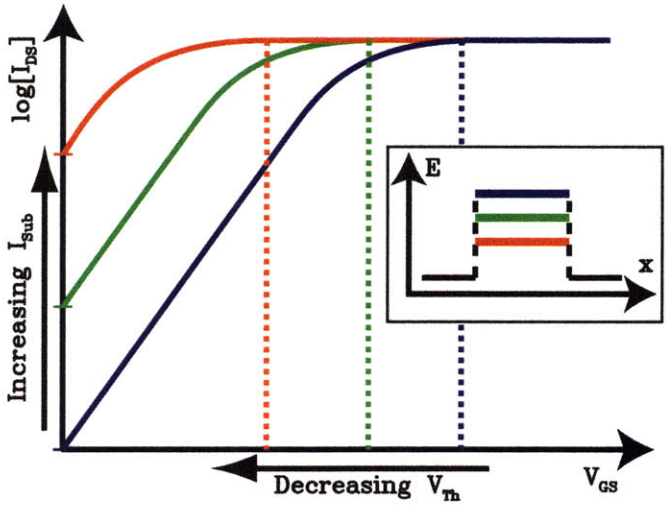


Figure 1-8: Plot of the source-drain current as a function of gate-source bias for various V_{th}.

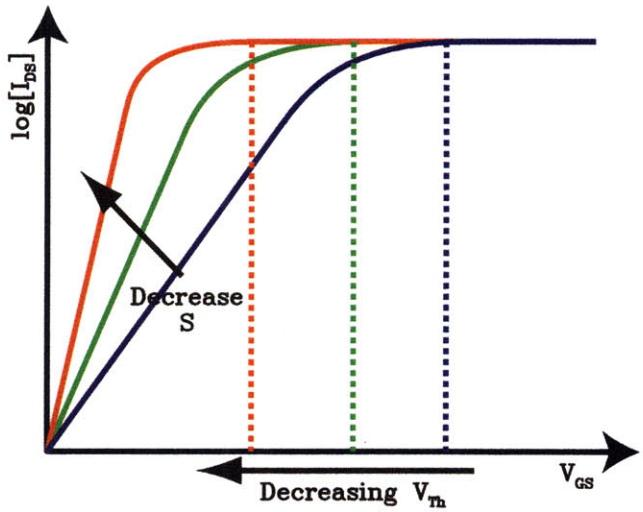


Figure 1-9: Plot of the source-drain current as a function of gate-source bias for various S.

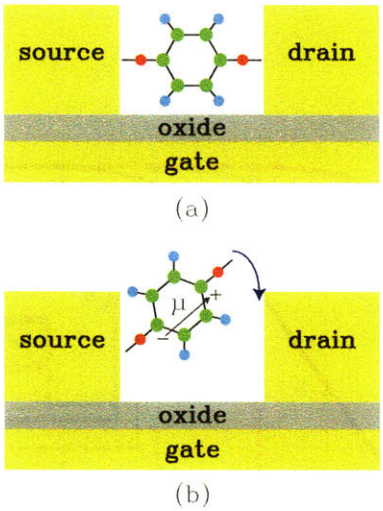


Figure 1-10: Comparison of a) conventional single molecule FET to that of a b) mechanical single molecule FET

the fundamental limits in power dissipation to computational logic in general. The minimum energy dissipated per bit will be briefly considered from a statistically mechanics arguments. Considering the use of binary logic, then the each bit used for computation can exist in one of two 2 states, either 0 or 1. Thus, a change in entropy of a single bit is given by $S = k_b \ln(2)$. Thus, the minimum switching energy per bit in any logic device is given by Equation 1.11 for any device including both NEM devices and conventional field effect transistors (FETs).

$$E_{\min} = k_B T \ln(2) \tag{1.11}$$

This the limit is known as the Shannon-von Neumann-Landauer (SNL) limit. [73] This highlights the fact that the limits in power dissipation in CMOS are not fundamental to the limits in power dissipation to computation, but limited to CMOS alone.

1.3 Case for NEMs

1.3.1 General Theory

In their theoretical work, Ghosh et al. [18] considered the limits of transconductance, and hence power dissipation, on the molecular scale, what some would consider the ultimate end of the roadmap in terms of scaling. From Equation 1.11, it is apparent that the scaling limits in CMOS power dissipation are limits in the design and architecture of electrostatically operated device, and therefore it was considered that any device that was electrostatically actuated would have the same limits. Therefore, a molecular device like the one in Figure 1-10a, whose current I is modulated by induction of charges via a gate voltage, V_g will, at best, have transconductance per unit current, g_m/I, of:

$$\frac{g_m^{es}}{I} = \frac{q}{kT} \tag{1.12}$$

Where q is the electron charge which, again, is the limit of a standard FET transconductance obtained in Section 1.1.3.2.

It is logical then to consider devices that operate by alternative means, such as mechanical actuated transistors. Let a device now be considered whose current is modulated by a gate voltage, V_g, induced conformational change like the one in Figure 1-10b, where the gate field interacts with the molecular dipole, μ, the transconductance per unit current, is now at best:

$$\frac{g_m^{conf}}{I} = \frac{1}{kT} \cdot \frac{\mu}{t} \tag{1.13}$$

where t is the length of the molecule. For a molecular dipole where there is no net molecular charge, the term $\mu/t = q$, meaning that equation 1.13 becomes:

$$\frac{g_m^{conf}}{I} = \frac{q}{kT} = \frac{g_m^{es}}{I}$$

This means that for no net molecular charge, there is no major benefit to me-

chanical transistors. This does not mean that from even this stand point mechanical transistors are not of interest, since they still offer an alternate route towards achieving the limits of transconductance.

1.3.2 Potential Solution

Since there is no net benefit to mechanical transistors when there is no net charge, what happens in the case where there are a surplus of charges? An archetype mechanical transistor, shown in Figure 1-11, consisting of a conducting actuator, which acts as a conventional channel, that is brought in and out of contact between the source and drain via a gate-field induced conformational change is considered for this discussion. In the case of a simple dipole, Figure 1-11a, the mechanical actuator is turned from the "off" to "on" positions by an applied bias threshold V_T or V_G. The difference in energy between the two positions is just qV. The subthreshold slope limit is thus the same for this device and a MOSFET. Now consider a device that moves between the same two energy states as before, but instead of moving a single charge, there are now three charges that need to be moved, Figure 1-11b. Because the energy difference in the two devices are the same, i.e. $\Delta E_{1-chg} = \Delta E_{3-chg}$, then $V_{th,3chg} = \frac{1}{3}V_{th,1chg}$ meaning the subthreshold slope of the mechanical device with three charges is $\frac{1}{3}$ that of a device containing 1 charge, or that of a MOSFET. This same idea can be applied to a system with Z charges, allowing for subthreshold slope decreases by a factor of $\frac{1}{Z}$. Conceptual this is very promising, but are there any devices or systems where this actually occurs, i.e. where multiple charges lead to a reduction in subthreshold slope? The answer to this question is found in biology in the form of voltage-gated ion channels.

1.3.3 Ion Channels

Voltage-gated ion channels are transmembrane ion channels that open through mechanical actuation of their voltage sensing helices by an applied bias across the membrane that enables the flow of ions through the channel. These systems provide a

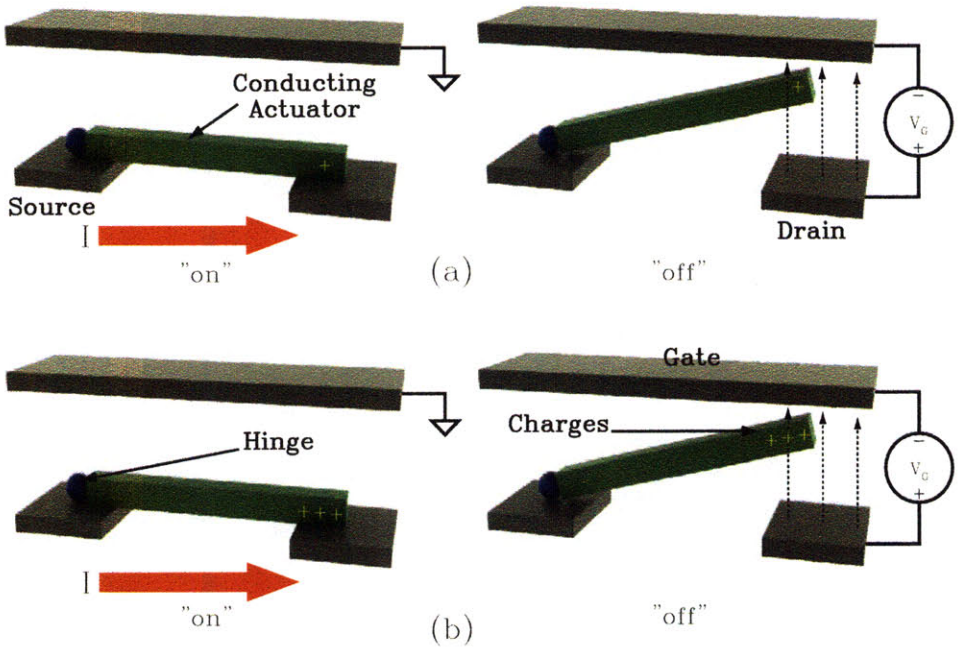


Figure 1-11: Mechanical Relay

system to investigate the influence of multiples charges for low voltage switches due to the fact that the helices themselves contain multiple positive charges that enable extremely low operating voltages. A schematic and diagram of a voltage gated potassium ion channel is shown in Figure 1-12. [30] The conductance versus voltage data for these voltage gated ion channels is shown in Figure 1-13. [23] Indeed, ion channels are able to switch with subthreshold slopes of 15 mV/decade, 4 times less than the 60 mV/decade limit of MOSFETs. This evidence shows the ability of multiple charges employed in an electromechanical based system towards the creation of devices that that exhibit low subthreshold slopes..

1.4 Our approach to address these problems

The purpose of this thesis is to create a test bed device for mechanical transistors with the future goal of being used to create devices that exhibit these low subthreshold swing switching characteristics.

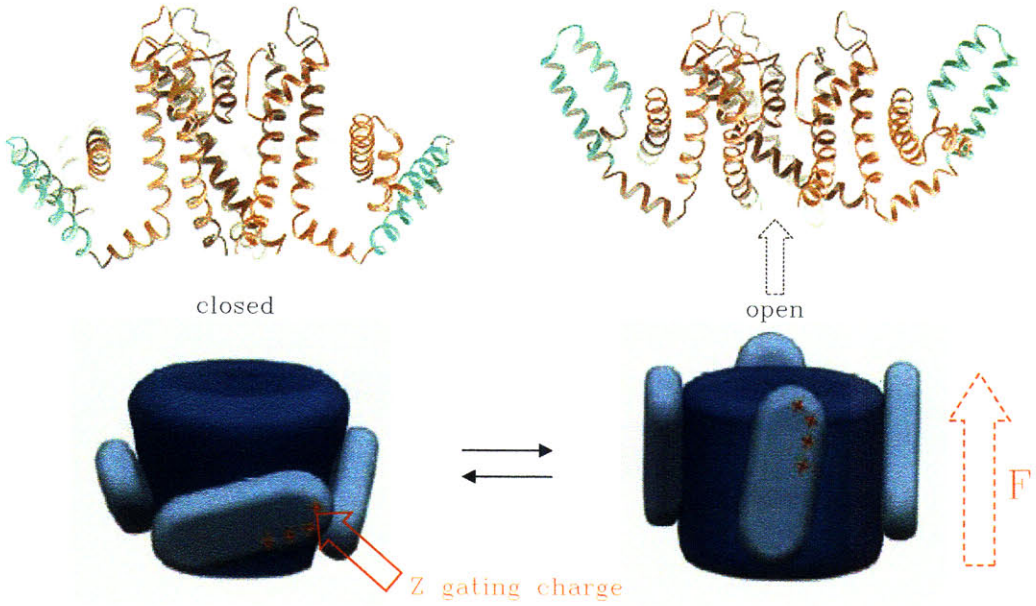


Figure 1-12: Voltage dependent K+ channel

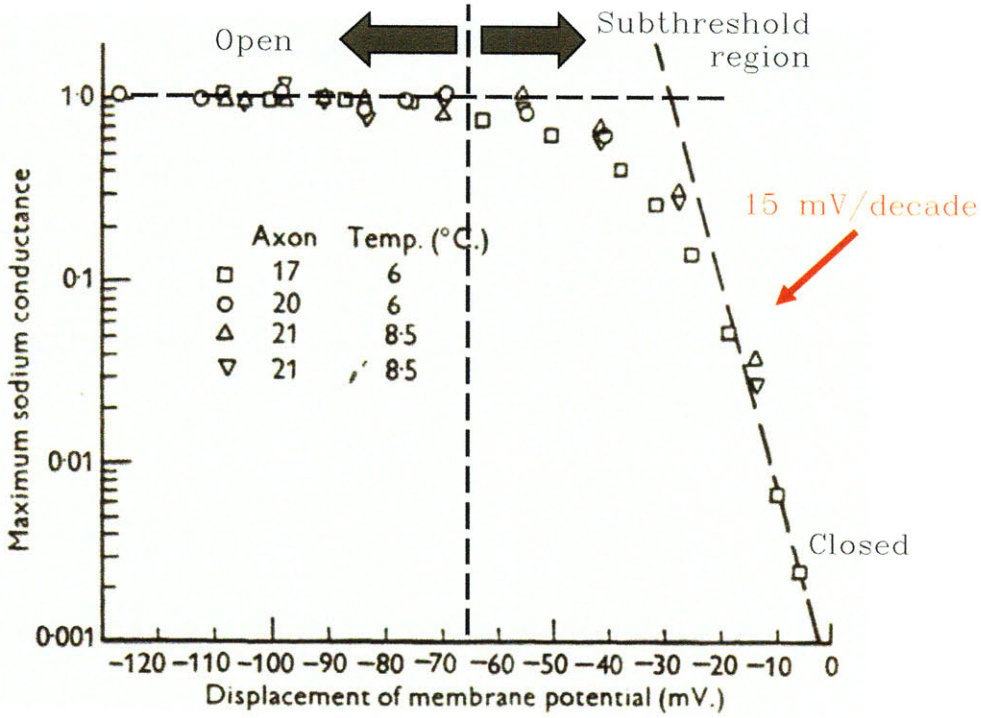


Figure 1-13: Data for a voltage gated ion channel. Hodgkin and Huxley, J. Physiol. 116, 449 (1952a)

1.4.1 Carbon Nanotubes

The most important consideration in creating a mechanical transistor is the selection of the material for the conducting actuator. In order to ensure a large on-off ratio the actuator needs to be highly conductive. Mechanically, the actuator needs to be able withstand multiple switching events without failure and therefore needs to be a very strong materials. Since it is desired to have a high integration density, the material should have both of these properties while having the physical size at the molecular scale. With the desire of creating a device that has multiple charges like an ion channel in the future, using a material that is functionalizable is highly desired.

Carbon nanotubes/fibers (CNs) are promising as a material for NEMs because of their exceptional and unique electronic, mechanical, and chemical properties. Essentially CNs are rolled sheets of graphene formed to create a tube, hence the name carbon nanotube, Figure 1-14. Their diameters can range from 2-300nm making them compatible with modern and future MOSFET integration. Electrically, CNs are highly conductive and can carry an electrical current density of $\sim 4 \times 10^9 \mathrm{Acm}^{-2}$, several orders of magnitude greater than that of copper or aluminum.[24] Mechanically, with a Young's Modulus ranging from 0.8 to 1 TPa, carbon nanotubes are the strongest known material. [68] Finally, opening up the ends of CNs in an oxidizing environment allows them to be functionalized with a large library of carboxyl (COOH) functional groups.[67]

In addition to all this, they have been well studied in terms of their synthesis [63] and have been used to create electromechanical devices such as actuators [3], tweezers [36], and even memory elements [59]. Hence, carbon nanotubes/fibers are the ideal candidate for NEM switches.

1.4.2 Device

The proposed device that's investigated in this thesis is a vertically oriented carbon nanotube/fiber (CN) based relay (VOCNR) shown in Figure 1-15. The device consists of a vertically oriented CN based actuator that is electrically connected to a substrate.

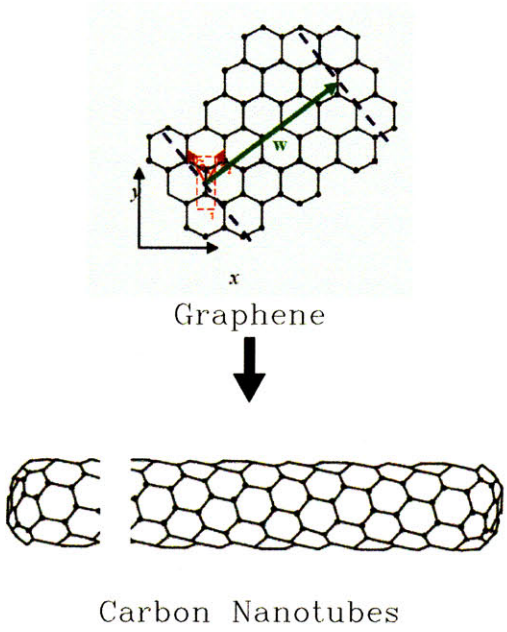


Figure 1-14: Structure of a carbon nanotube from a sheet of graphene.

Situated on either sides of the CN are contacts that are electrically isolated from each other as well as the CN. A schematic of the device under operation is shown in Figure 1-16. The envisioned as grown device begins with the CN mechanical actuator situated in the center of the two contacts, Figure 1-16a. A bias is applied between the CN and one of the contacts and the device is turned on when the voltage is large enough to pull the CN into electrical connection with the contact, the voltage at which this occurs in the pull-in voltage, V_{pi}, Figure 1-16b. The CN then remains connected to the contacted because of small scale van der Waals forces, Figure 1-16c. An bias applied between the CN and the opposing contact turns the device off when the device is pulled into the opposing contact, the voltage at which this occurs is the pull-off voltage, V_{po}, Figure 1-16d.

1.5 Thesis Overview

In Chapter 2 the theory and design of the VOCNR are discussed. First, a basic continuum model of these relays is examined in order to understand device scaling as it relates to the pull-in voltage. After understanding the basic operating principles

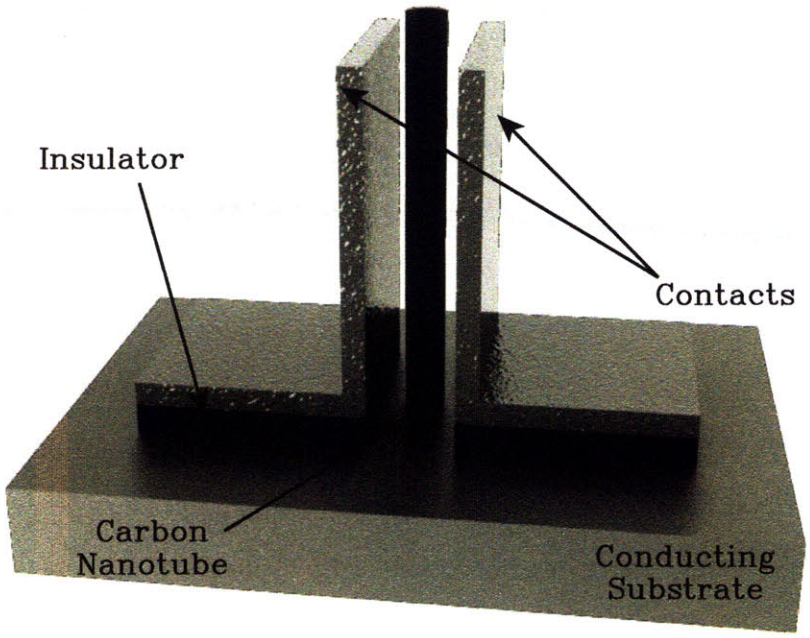


Figure 1-15: Proposed device for studying nanoelectromechanical systems

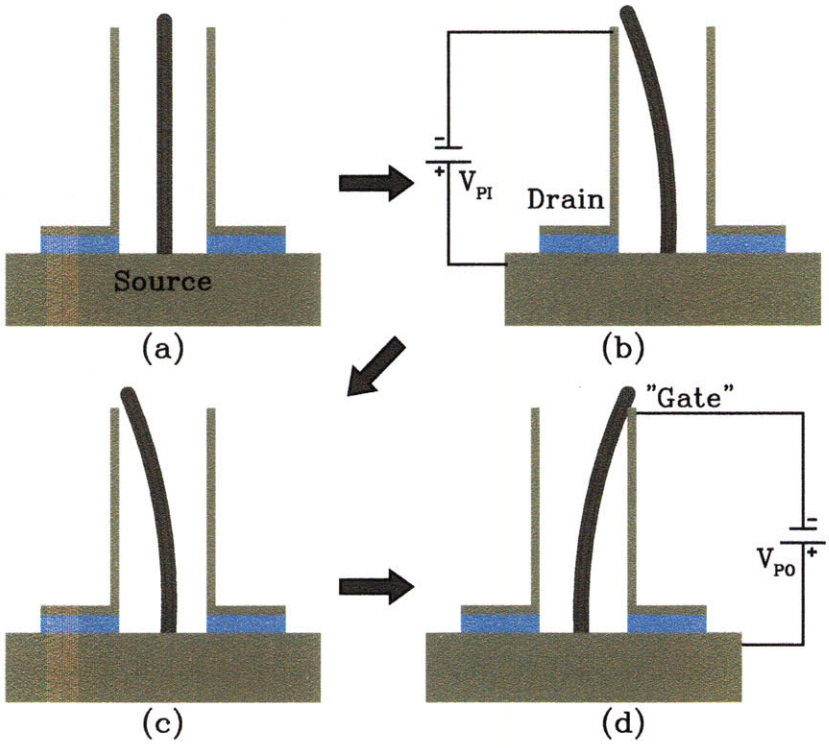


Figure 1-16: Operation of a Vertically Oriented Carbon Nanorelay

of the device the issues as they are related to previous works in this area are looked at, in particular is the issue of stiction in NEMs. Last, are the ways these issues are addressed by the design of a NEMs relay presented in this thesis.

In Chapter 3 the initial prototyping and first generation fabrication efforts are discussed. First, an overview of the first generation architecture and fabrication route to a vertically oriented carbon nanorelay is given. The virtues of the architecture and fabrication in terms of performance criteria as well as potential pitfalls are also given. Second, a proof of concept experimental setup is described and the results are given. Last, a set of experiments utilizing the proof of concept setup and initial fabrication efforts is described followed by results and a discussion.

In Chapter 4 a fully wafer integrated vertically oriented or vertical carbon nanorelay is discussed. Fabrication issues such as limitations in nanotube and oxide growth via PECVD are examined. A novel self-aligned technique for creating precisely aligned gaps to vertical structures is presented. Results are analyzed to demonstrate device scaling. Finally, pull-in data for a device is shown and related to limitations in fabrication.

In Chapter 5 a new type of electromechanical switch fabricated from two layers of graphene films grown via ambient pressure chemical vapor deposition also called a double graphene switch is discussed. This includes the design and fabrication of the device as well as the electrical and electromechanical characterization of the double graphene. Finally the failure of the device due to mechanical tearing of the graphene is shown.

In Chapter 6 conclusions regarding both a vertical carbon nano-relay and a double graphene switch are presented. This is mainly meant to highlight some of the virtues as well as pitfalls in the overall work in this thesis.

Finally, in Chapter 7 future avenues of suggested research for both devices are presented. This includes, but is not limited to, the optimization of the vertical carbon nanorelay for wafer integrated pull-off operation and the scaling the double graphene switch to enhance the mechanical robustness of the device.

Chapter 2

Theory and Design

2.1 NEMs Relay: Continuum Model

The continuum modeling of a CN based NEMs relay follows from the works of Desquenes et al. [12] A complete and in-depth model for CN based relays can be found in a variety of references. [12, 37, 13, 71, 21] In large part these models are validated by considering how they compare to molecular dynamics models and few experimental devices, and have shown good correlation between the both. In general the difficulty in modeling NEMs is not the accuracy of the model, but in the wide variations in the properties of the nanostructures they are modeling. As an examples, the elastic modulus of carbon nanotube and nanofibers can vary by upwards of about two orders of magnitude depending on, amongst other characteristics, the diameter [60, 41], structure [39], and growth method [46]. In this thesis only a basic model involving the static behavior, or more specifically the pull-in behavior, of carbon based NEMs will be considered for the purpose of understanding device scaling. As such, the validity of a continuum mechanics model for the primary device of this thesis, the vertical carbon nano-relay, will be partially proven by considering the scaling behavior of a measurable parameter, such as gap size, of a single device (Section 4.3.1).

Although the analysis will primarily focus of vertical carbon nano-relays with a cantilever type structure, schematically shown in their "on" and "off" states in Figure 2-1a and 2-1b, respectively; the analysis technique can also apply to relays

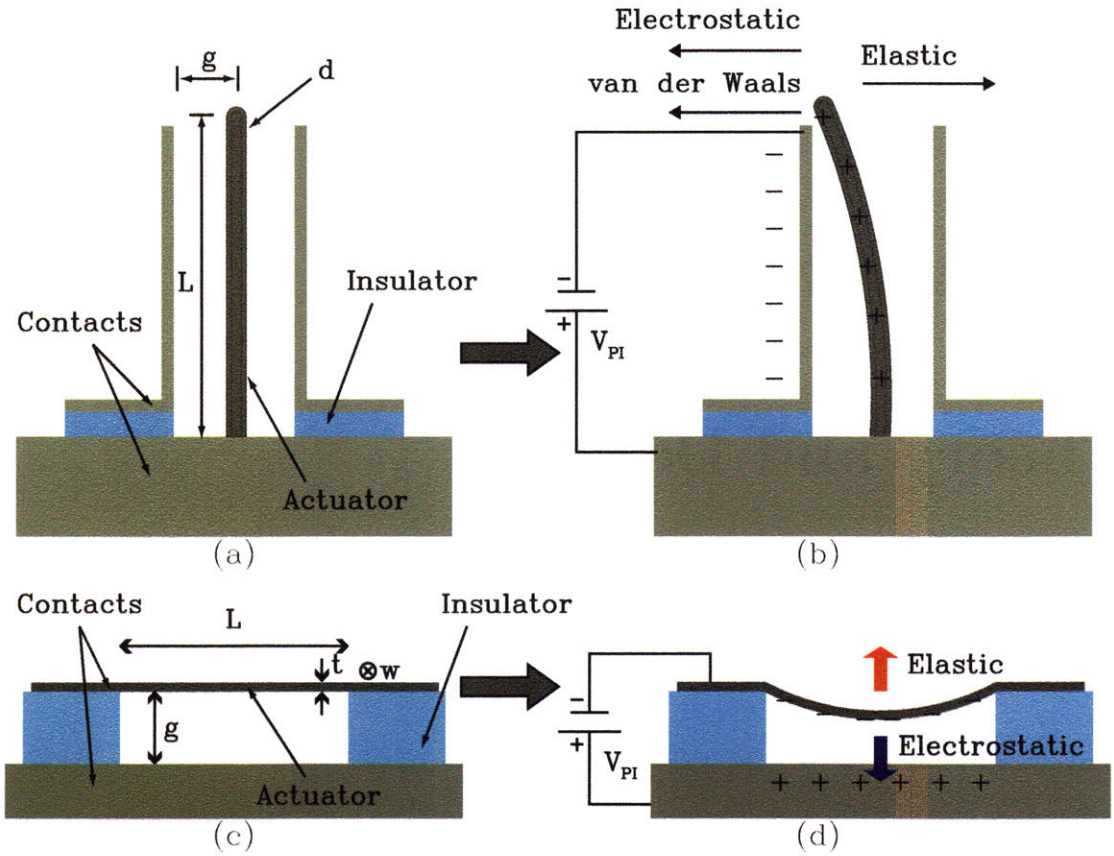


Figure 2-1: Forces involved in a carbon nano-relay. Schematic of: a) an vertical carbon nano-relay showing relevent dimensions. b) an activated vertical carbon nanorelay showing relevent forces. c) a horizontal beam relay showing relevant dimensions and d) an activated horizontal beam relay showing relevent forces

that are dual clamped as in a horizontal beam device schematically shown in their "on" and "off" states in Figures 2-1c and 2-1d, respectively. The basic principle to solving the static behavior of a CN based relay is a simple balance of forces when either device is actuated by an applied bias. When a bias is applied between the CN cantilever or possibly even a graphene beam and an electrode several forces act on the electromechanically actuating the cantilever or beam. There are electrostatic and to a lesser extent van der Waals forces that cause deflection of the actuator towards the conducting electrode and elastic restoring forces opposing the deflection of the beam. In addition, the analysis will consider both the case of MWCNT or large carbon nanofibers with cylindrical cross sections with outer diameters, d, as well as the case of a graphene sheet with a width and thickness of w and t respectively.

2.1.1 Van der Waals

The van der Waals interaction between the CN and the contact is modeled by the Lennard-Jones potential [44]

$$\varphi_{ij} = \frac{V_R}{r_{ij}^{12}} - \frac{V_A}{r_{ij}^{6}} \tag{2.1}$$

where r_{ij} is the distance between ith and jth atoms, V_R is the repulsive constant, and V_A is the repulsive constant. By following the model in by Desquenes et al. [12] The van der Waals interaction force can be written as:

$$F_{vdW} = -\frac{\pi V_R \rho^2 w L}{6}\left(\frac{1}{g^3} - \frac{1}{(g+t)^3}\right) \tag{2.2}$$

for a rectangular beam, or

$$F_{vdW} = -\frac{\pi V_R \rho^2 d L}{6}\left(\frac{1}{g^3} - \frac{1}{(g+d)^3}\right) \tag{2.3}$$

for a cylindrical beam, where ρ is the atomic density, L is the length of the actuator and g is the gap size. Although the van der Waals forces are written here for completeness, they will be ignored in the final analysis, because of their insignificant contribution to pull-in which occurs at relatively large gap sizes, $g_{pull-in} = \frac{2}{3}g_i$, where g_i is the initial gap size, [61] as well as the relatively large size CNs used in this thesis.

2.1.2 Electrostatic

The electrostatic or capacitive force is easily derived by considering the electrostatic force, F_{s_elec}, felt by a single charge, q, in electric field, E, is written as

$$F_{s,elec} = qE \tag{2.4}$$

Then for a device with multiple charge, Q, in an electric field the total electrostatic force, F_{elec} is equal to

$$F_{elec} = QE \tag{2.5}$$

If in either case of an beam or a cantilever the device acts like a parallel plate capacitor, that the total number of charges Q on the capacitor is given as:

$$Q = \frac{\varepsilon_0 A_C V}{g} \tag{2.6}$$

where ε_0 is the permittivity of free space, A_C is the area of the capacitor, and V is the applied voltage. The electric field is written as:

$$E = \frac{V}{g} \tag{2.7}$$

Combining Equations 2.5,2.6, and 2.7 the following equation is derived for the electrostatic force:

$$F_{elec,cy} = \frac{1}{2}\frac{\varepsilon_0 A V^2}{g^2} \tag{2.8}$$

Again for simplicity, assume that a cylinder has more or less the area of a rectangle, then:

$$F_{elec,re} = \frac{1}{2}\frac{\varepsilon_0 d L V^2}{g^2} \tag{2.9}$$

and for a rectangular beam:

$$F_{elec} = \frac{1}{2}\frac{\varepsilon_0 w L V^2}{g^2} \tag{2.10}$$

2.1.3 Elastic

In it's equilibrium state a beam or cantilever remains in an undeflected state, therefore in order to deform that beam or cantilever an elastic force related to the spring constant, k, and deflection distance Δg must be applied in order to deform the beam. Since every action has an equal and opposite reaction, the equal and opposite reaction

is the elastic repulsive force and is given by:

$$F_{elas} = k\Delta g \tag{2.11}$$

The spring constant, k, depends on the material and geometry of the actuator. For a cantilever type device the spring constant is given as:

$$k_{can} = 8\frac{EI}{L^3} \tag{2.12}$$

and for a double clamped beam the spring constant is:

$$k_{beam} = 384\frac{EI}{L^3} \tag{2.13}$$

where E is the modulus of elasticity and I is the moment of inertia. Again, the moment of inertia is a function of the geometry of the beam and is defined for a cylinder as:

$$I_{cy} = \frac{\pi d^4}{64} \tag{2.14}$$

and for a rectangular prism as:

$$I_{re} = \frac{wt^3}{12} \tag{2.15}$$

The following equations are obtained for the elastic forces of a cantilever with cylindrical cross section:

$$F_{elas,can,cy} = \frac{\pi d^4 E}{8L^3}\Delta g \tag{2.16}$$

and for a beam with a rectangular cross section:

$$F_{elas,beam,re} = \frac{32wt^3 E}{L^3}\Delta g \tag{2.17}$$

2.1.4 Pull-In Scaling

Pull-in occurs when $F_{elec} = F_{elas}$ for a gap[61]:

$$g_{PI} = \frac{2}{3} g_i \tag{2.18}$$

By the above equations for various geometries the following relations are obtained for the pull-in voltage, V_{PI}, as a function of the geometry of the actuator and gap size, for a cylindrical cross section

$$V_{PI,cy} \propto \sqrt{\frac{Ed^3g^3}{L^4}} \tag{2.19}$$

and for a rectangular cross section:

$$V_{PI,re} \propto \sqrt{\frac{Et^3g^3}{L^4}} \tag{2.20}$$

Equations 2.19 and 2.20 provide general guideline for device design as it relates to scaling of the operating voltage of a nanorelay.

2.2 Previous Approaches

Several approaches have been implemented in discovering a route towards a carbon nanotube/fiber based NEMs. Although each approach has been successfully employed, limitations in their design and fabrication prevent them from being a practical replacement for CMOS. The issues of these designs thus far has been stiction, both in the creation of a horizontal and vertical design, and finally alignment of contacts with respect to the carbon nanotube. Of these two flaws, stiction is the most crucial as it is a fundamental problem, rather than a limitation in fabrication, and will be reviewed in Section 2.3.

2.2.1 Horizontal 3-Terminal CNT Relay

One of the earliest CNT based NEMs was a horizontally oriented, three terminal relay created by Lee et al [42] at Gteborg University and Chalmers University of Technology. A schematic of their design is shown if Figure 2-2 and is comprised of a horizontally oriented multiwall CNT fixed at the source electrode (S) and suspended over a gate (G) and drain (D) contact. The switch is turned on when a bias is applied between the source and gate causing capacitive forces to pull the tube down towards the drain contact. Eventually the tube comes into contact, or at least close to, with the drain contact allowing current to pass from the source to the drain. When the gate voltage is subsequently turned off the tube is released and the contact is broken, i.e. the device is turned OFF. Figure 2-3a shows a "typical" I-Vsg curve for one of these devices. In these "typical" devices the carbon nanotube is mechanically actuated and brought into close enough distance to allow current to tunnel from the nanotube to the drain contact but is never brought into mechanical contact to the drain electrode. It was speculated absorbate layer on the surface of the nanotube prevented direct mechanical contact from the nanotube to the drain electrode. The lack of physical contact allows the tube to operate reversibly for at least two consecutive runs, but the device suffers from very low on currents. There were also a set of devices that apparently did not have this speculated absorbate layer and in these devices the nanotube was able to come into mechanical contact with the electrode, but with catastrophic results. When the nanotube does come into mechanical contact with the drain electrode the on current is, of course, much higher (Figure 2-3b) but the nanotube remains in contact with the drain even one the bias is removed. This failure as a result irreversible mechanical actuation of the nanotube to the drain electrode highlights one of the biggest flaws in this device, and in many NEMs devices, of failure due to stiction. A device that suffered from stiction based failure is shown in Figure 2-3b.

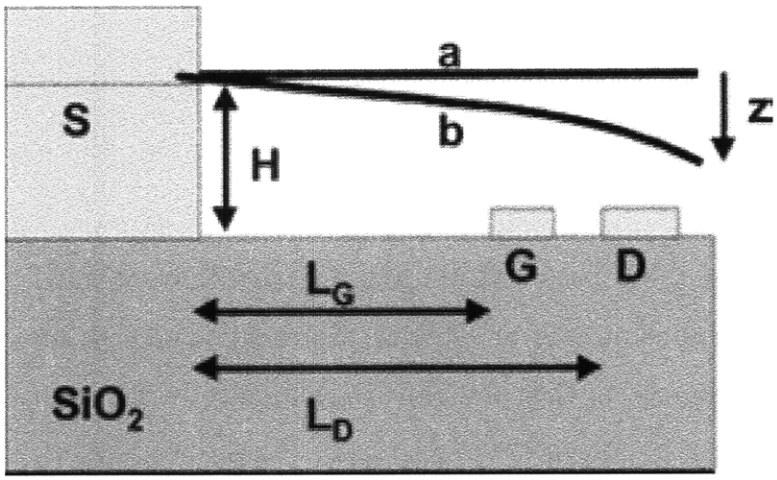


Figure 2-2: Horizontal 3-Terminal CNT Relay

2.2.2 Vertical 3-Terminal CNT Relay

The second attempt at making a viable CNT based NEMs switch was by Jang et al at the University of Cambridge. [28] [27] In their works on CNT switches they looked at several vertically based architectures. One using three vertically oriented CNTs (Figure 2-4b), the second using two CNTs (Figure 2-4c), and the third is an application of the two CNT device as a switch capacitor (Figure 2-4a). All devices are three terminal devices comprising of a drain, source, and gate in the first case all of these are nanotubes and in the later cases there is a drain and source nanotube and an adjacent gate contact. Both operate in a similar fashion. Initially a small bias is applied between the drain and source tubes causing a buildup of positive static charges to occur on the drain tube. By applying a positive bias to the gate tube/contact the drain tube is eventually "pushed" into contact due to the repulsive forces between the gate and the drain. The three-tube device is shown in Figure 2-5 along with the current-voltage characteristics of the same three terminal device. As in the case with the device created by Lee et al, the device fails after a single run as a result of stiction between the two nanotubes. The group was able to create a two tube device that at least operated for several runs by decreasing the aspect ratio of the tubes. By decreasing the aspect ratio of the nanotube the restoring elastic forces were increased high enough to overcome the stiction forces keeping the tubes together.

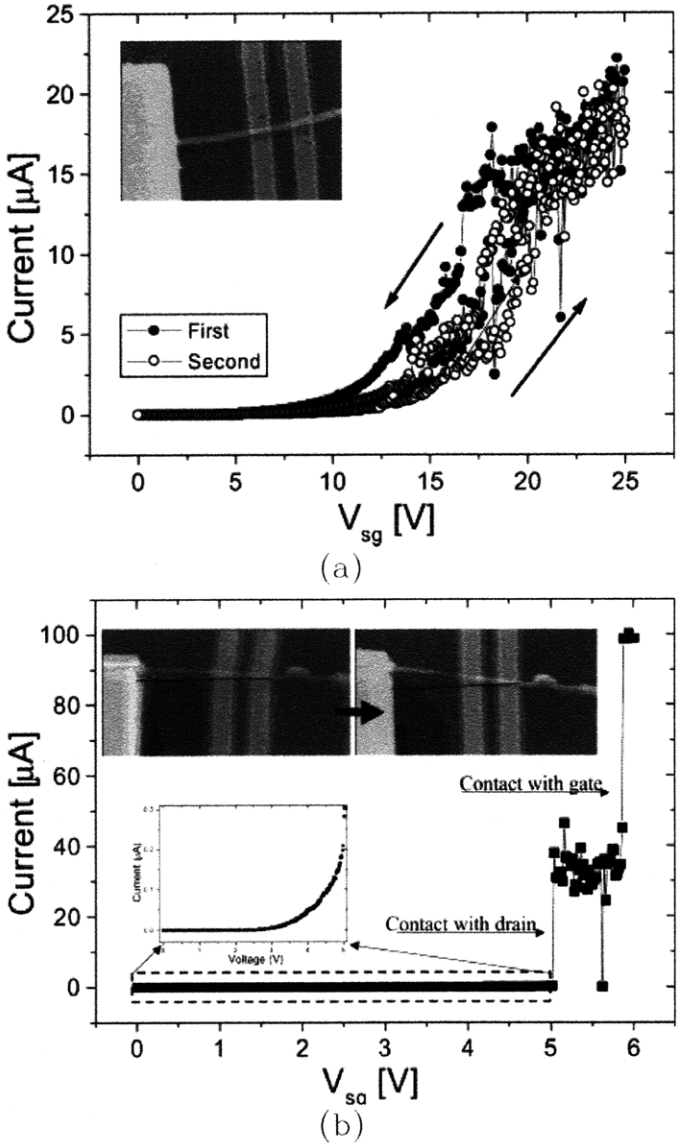


Figure 2-3: Data for Horizontal 3-Terminal CNT Relay in a) non-contact mode allowing for at least two iterations and b) contact mode where the device suffers from stiction to the contacts

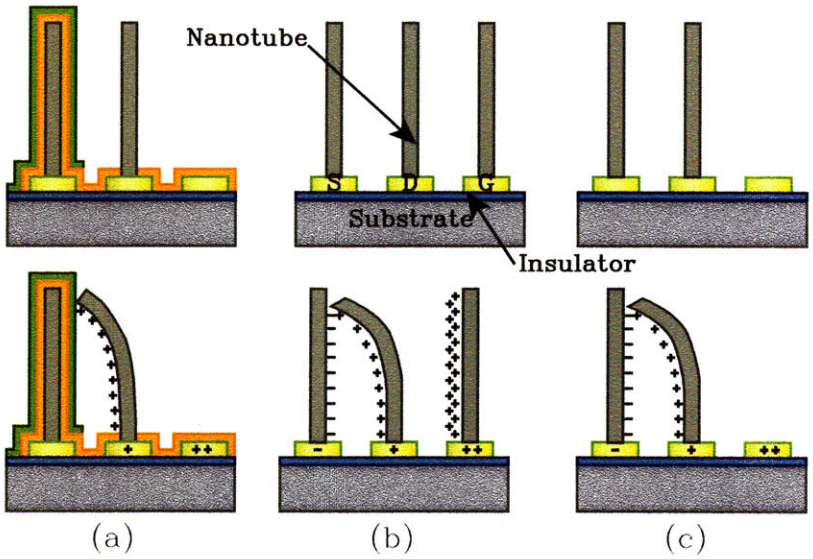


Figure 2-4: Example of several different devices built by the Cambridge group. Shown Top: As fabricated and Bottom: Under activation

Two two-carbon nanotube device are shown in Figure 2-6, the first device operated a single run due to van der Waals forces, Figure 2-6a, and the second was able to run several times, Figure 2-6b, the I-V curves for the two devices show an increase in actuation voltage with the smaller aspect ratio tubes. These results highlight one of the fundamental issue in these type of "three" terminal NEMs devices, that the ability to create a device to withstand multiple operations without stiction comes at the cost of high operating voltages.

2.2.3 Vertical 3-Terminal CNT Relay with Pull-Off

The latest attempt in creating a nanotube based switch comes from Kaul et al at the Jet Propulsion Laboratory. [32] A schematic of their proposed device is shown in Figure 2-7a. Similar to the device created by Jang et al, the device also implements a vertically grown carbon nanotube. Rather than using a second nanotube and a bottom terminal gate, the device uses a single carbon nanotube oriented between two contacts. The device is fabricated by starting off with a heavily doped silicon substrate with a layer of oxide. A growth pocket is created by etching a hole in the oxide layer and a catalyst for nanotube growth is deposited on the bottom. After

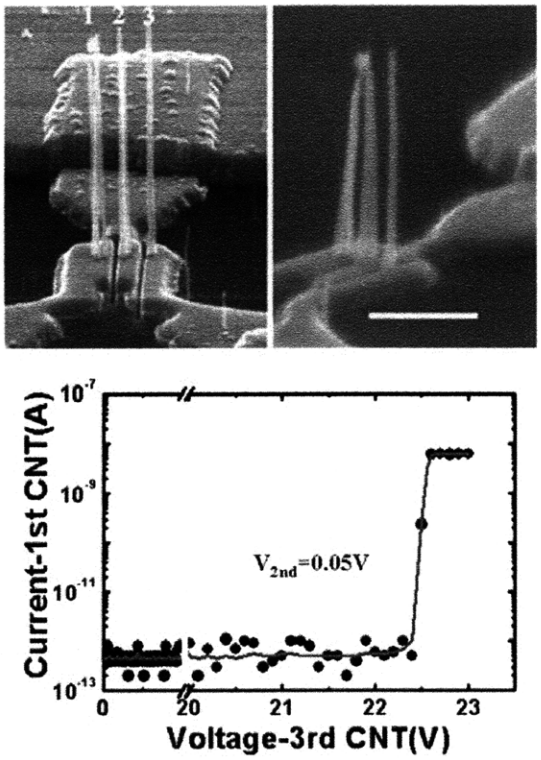


Figure 2-5: Top Left: Scanning electron micrograph of an as fabricated three-carbon nanotube switch. Top Right: SEM micrograph of the same device after the removal of an applied bias. The scale bar corresponds to 1 μm. Bottom: Current versus voltage characterstics.

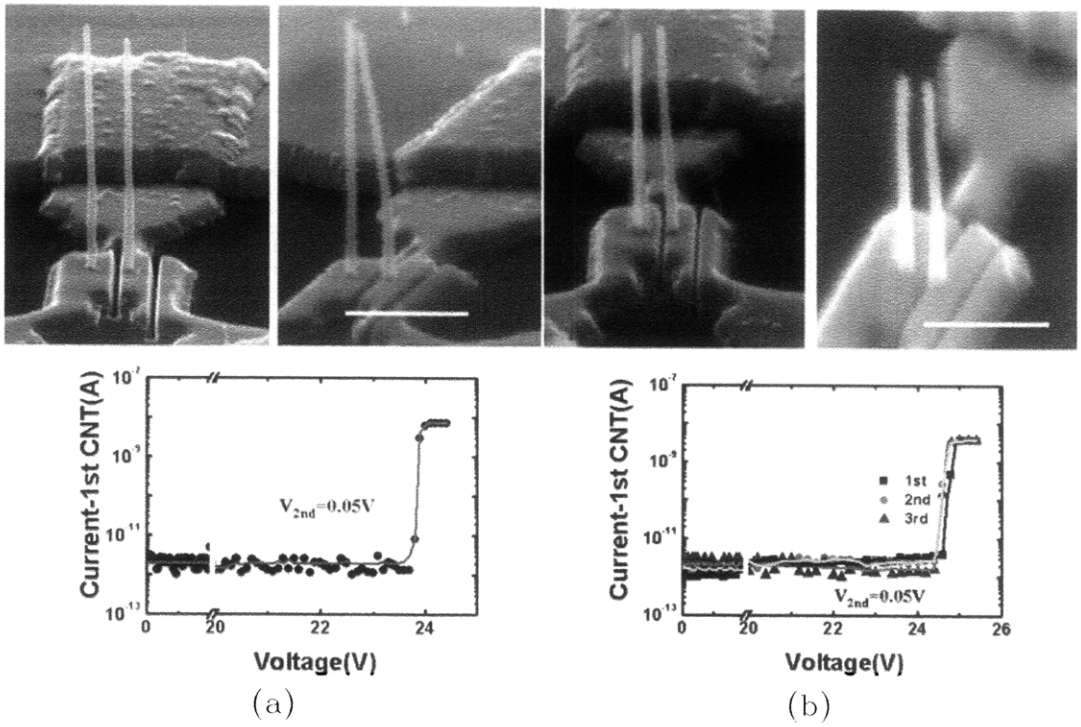


Figure 2-6: Two two-carbon nanotube switches that were tested. a) Device made with high-aspect ratio tubes Top Left: Scanning electron micrograph of an as fabricated two-carbon nanotube switch. Top Right: SEM micrograph of the same device after the removal of an applied bias. The scale bar corresponds to 1 μ Bottom: Current versus voltage characteristics. b) Device made with low-aspect ratio tubes

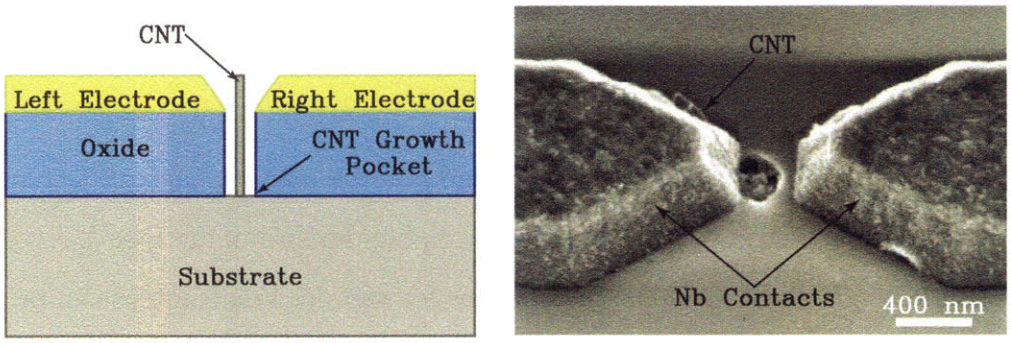


Figure 2-7: a) Schematic of a vertically oriented carbon nanotube relay created by the group at JPL b) Scanning electron micrograph of the device. [32]

their masking layer is removed a set of niobium contacts are deposited on top of the substrate. The final step in their process is the growth of the tube, and the results are shown in Figure 2-7b. Besides the fabrication there have been no reports of testing of the device.

2.3 Stiction

In the field of NEM/MEMs devices stiction is one the most common reasons for device failure. Stiction is defined as the of the the irreversible adhesion of an actuating structure as a result of short range forces experienced during mechanical contact with another surface. Upon contact, short range forces such as capillary forces, van der Waals forces, electrostatic attraction, and even direct chemical bonding forces dominate over restoring elastic forces. This is especially critical in NEMs switches where achieving low voltages requires low restoring elastic forces. This is evident when looking at devices in Sections 2.2.1 and 2.2.2 where stiction causes instant failure of the devices upon first contact. A model for these forces was first analyzed by Maboudian and Howe in 1997. [47] Although these models for "predicting" stiction forces in MEMs are available, they show very poor correlation to acutal experimental data[65], but will be discussed for completeness nonetheless.

Capillary forces arises from surface tension of water at the interface between the actuator and surface. Then the work of stiction by capillary forces is given as:[47]

$$W_{cap} = 2\gamma_l \cos\theta \tag{2.21}$$

where γ_l is the surface tension of water and θ is the contact angle of water.

Van der Waals stiction forces arise from dipole-dipole interactions between the actuator and the contact surface. The analysis for van der Waals forces can be found in Section 2.1.1. Ultimately the best way to determine the surface interaction energies is to measure them by creating an array of cantilevers with varying length, width and gap size and to measure the amount of contact between the actuators and contact surface. [11]

The same electrostatic attraction that operates the actuator can also lead to stiction. Electrostatic attraction based stiction between the actuator and a contact surface is primarily a problem when the surface itself is either a dielectric or coated with a dielectric to prevent stiction due to capillary stiction. When the actuator makes contact with the dielectric surface charges can transfer and remain embedded in the dielectric. Eventually enough charge can be built up such that the device stays "electrostatic actuated" despite the device being turned off. Thus the work of stiction by electrostatic forces is:[47]

$$W_{elec}(d) = \frac{\varepsilon_0 V^2}{2d}$$

where d is the gap distance, V is the potential differencem, and ε_0. Again, this is primarily a problem where dielectrics are concerned. Electrostatic attraction stiction is typically not a cause for concern for NEMs electrical switches, since most of the materials used are conducting.

2.4 Challenges and Design Requirements

In examining the previous work on horizontal and vertical CN switches there are several major challenges towards realizing a low voltage, reliable CN based relay that are addressed in the design of a vertically oriented carbon nanorelay presented in this

thesis.

Again, the leading problem in these devices and NEM/MEMs in general is failure due to irreversible switching, or stiction, [4] which arises primarily from small scale forces such as van der Waals forces and capillary forces. The solution to preventing stiction in these class of devices has been to either to: (i) create structures with large elastic forces to overcome the stiction forces, (ii) avoid direct contact and operate in the regime of tunneling, or (iii) coat contacts with an insulating material to prevent stiction and, again, operate the device by tunneling. Unfortunately these approaches result in either high operating voltages or low on current. Rather than trying to prevent stiction the design proposed in this thesis assumes that stiction will occur as part of the operation and utilizes a second opposing contact to "undo" stiction rather than prevent it. In this manner, a device can be operated without concern of stiction induced failure enabling both low operating voltage and high on current operation.

Based on the trend in Equation 2.19, in order to produce a device that can operate at low voltages a large aspect ratio is desired. The vertical design enables decreased voltages without an increase in device scaling as would be the case in a horizontal structure like the one created by Lee et al. [42] Furthermore, a vertical architecture capitalizes on the molecular size diameter of the tube to allow for large integration density.

Finally, in order to create an integrated device the contacts must be well aligned to the tube in order to minimize the gap size. One of the issues with the design by Kaul et al is their use of traditional alignment techniques. Alignment of these structures with one another is on the order of 10s of nanometers even using sophisticated techniques such as electron beam lithography. This issue is addressed with two different self-alignment techniques for alignment contacts to gaps and are presented in Chapters 3 and 4.

Chapter 3

Prototyping

3.1 Proof of Concept

Initially several proof of concept experiments were performed to determine whether or not a nanotube could be electrostatically pulled-in, something which has been shown before [36, 59, 55, 28, 32, 33, 9, 27] but was an important first step nonetheless and second, and most importantly, whether or not a pulled-in device could be pulled-off.

3.1.1 Testing Setup

The key component to the proof of concept work was the utilization of a Zyvex S100 Nanomanipulator installed on a JEOL JSM-6060 scanning electron microscope (SEM) shown in Figure 3-1. The Zyvex S100 consists of 3 individually controlled nanomanipulators to which tungsten (W) probes/tips are attached in order to make electrical contact with objects under the SEM. The probe can be manipulated to increments down to 5nm but the system itself is limited by the resolution of the microscope which is approximately 50nm. The tool is connected to a Keithley Model 4200-SCS Semiconductor Characterization System which allows current voltage measurements to be take in-situ under the SEM.

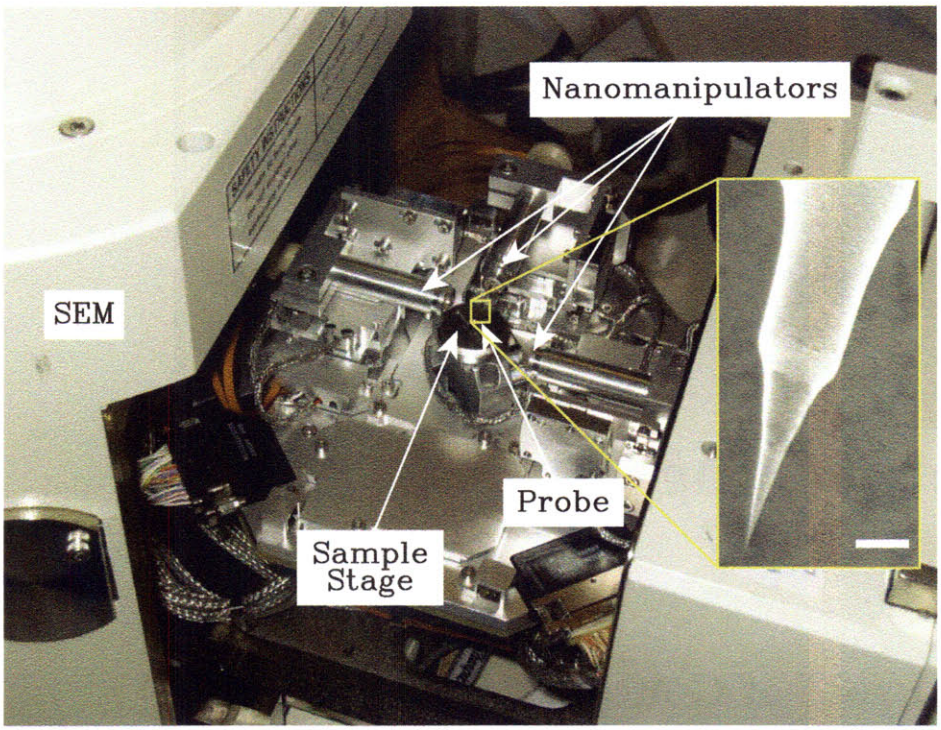


Figure 3-1: Photograph of the Zyvex S100 Nanomanipulator installed on a JEOL JSM-6060 SEM. The inset is a scanning electron micrograph of an etch tungsten wire probe for making electrical contact. The scale bar corresponds to 100 μm

3.1.2 Tube Attachment

In order to take CN based electromechanical measurements a carbon nanotube or fiber must first be electrically attached to the tungsten probes. Several techniques were utilized: van der Waals attachment [72], electron beam induced deposition (EBID) [52], and dielectrophoretic attachment [25].

3.1.2.1 van der Waals attachment

In this method a carbon nanotube or fiber is extracted from a forest of CN and attached to a tungsten probe simply using van der Waals forces. The tungsten tip is brought into contact with a single, isolated CN from a CN forest source. By manipulating the tip in such a way that the area of contact of the isolated CN with the tungsten tip is greater than that of the area of the contact of the isolated CN with other CNs in the forest a situation is created where the van der Waals forces between the isolated CN and the tip are greater than that of the isolated CN to the forest.

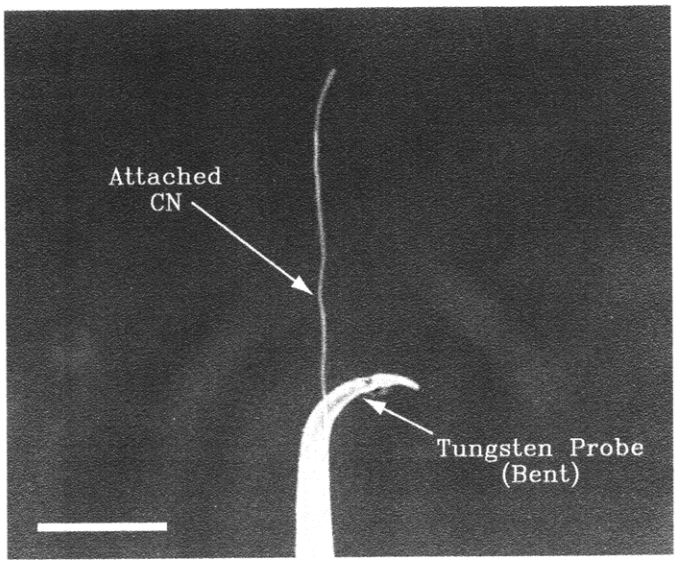


Figure 3-2: Scanning electron micrograph of CN attached to a tungsten probe using van der Waals attachment technique. The scale bar corresponds to 20 μm.

Once the tip is pulled away from the forest the isolated CN is then released from forest and remains attached to the tip, Figure 3-2. The CN forests themselves were grown from thermal CVD using a 75nm iron (Fe) catalyst source and were grown under [enter here], Figure 3-3a. The forests themselves are quite dense making it difficult to isolate individual tubes. Samples were cleaved in order to cause a section of the CN forest near the cleaved edge to collapse and make it easier to isolate individual CNs, Figure 3-3b.

3.1.2.2 Electron Beam Induced Deposition

Although the previous technique for tube attachment worked as evidenced by the SEM in Figure 3-2 most attempts to extract individual tubes using van der Waals attachment failed. EBID essentially involves the breakdown of a gas precusor with an electron beam and results in the the deposition of material containing elemental components of the precursor. In this particular case, oil from the diffusion pump used to pump down most SEMs, including the JEOL JSM-6060 used in these experiments, to high vacuums provided hydrocarbon molecules for the deposition of a carbonaceous material. [52] This method was employed to increase the attachment force of the CN to the tungsten probe by essentially welding the CN to the tube by depositing

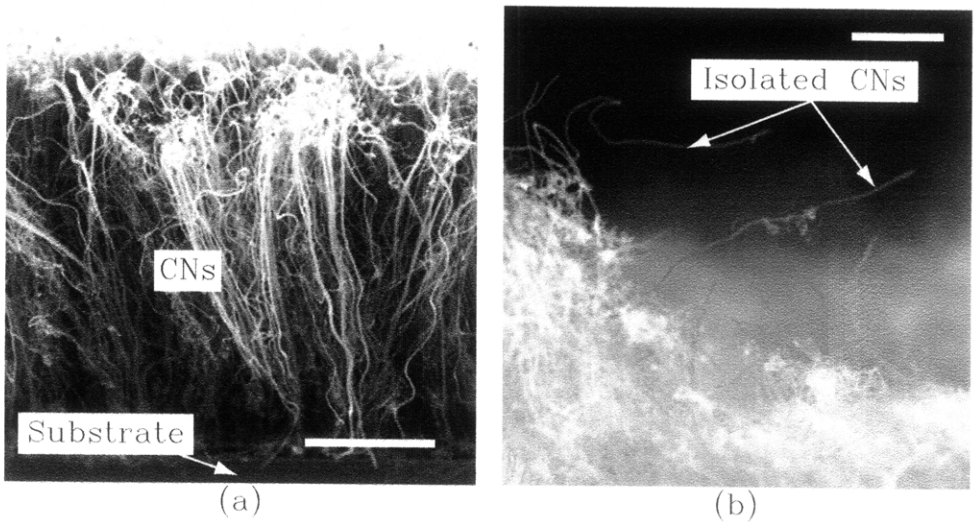


Figure 3-3: Scanning electron micrograph of a) cross-section of a forest of CNs grown via thermal CVD. The scale bar corresponds to 50 μm. b) top view of a cleaved section showing isolated CNs. The scale bar corresponds to 5 μm.

carbonaceous material at the tube-tip interface. Using an accelerating voltage of 10 kV, an aperture of 40 μm, and a magnification of 35000x a deposition rate of approximately 0.2-0.5 Å/min was achieved on the CN. Figure 3-4 is an example of a CN attached probe that was facilitated by EBID of about 20-30nm of material.

3.1.2.3 Dielectrophoretic attachment

Although the EBID enhanced van der Waals attachment of CNs described in the situation increased the yield of CN attachment to W tips, the slow deposition rate still hindered the ease of the CN attachment. Furthermore, often times a sample containing the CN forest would first be introduced into the chamber and then would have to be swapped out with a first generation test structure, to be described in Section 3.2, this reloading of a new sample often times resulted in the destruction of the CN. Dielectrophoretic attachment, involving the attachment of CNs to a tungsten tip from a CN solution, was used as a means for rapid attachment of CNs. A schematic of the DEP setup is shown in in Figure 3-5, exact details of the technique are described elsewhere.[25] Multiwalled carbon nanotubes (Cheaptubes) were dispersed N,Ndimethylformamide (DMF) by ultrasonication. An ac bias of 1 MHz with a V_{rms} bias of 6 V was applied between the tungsten tip and the CNT solution for 5

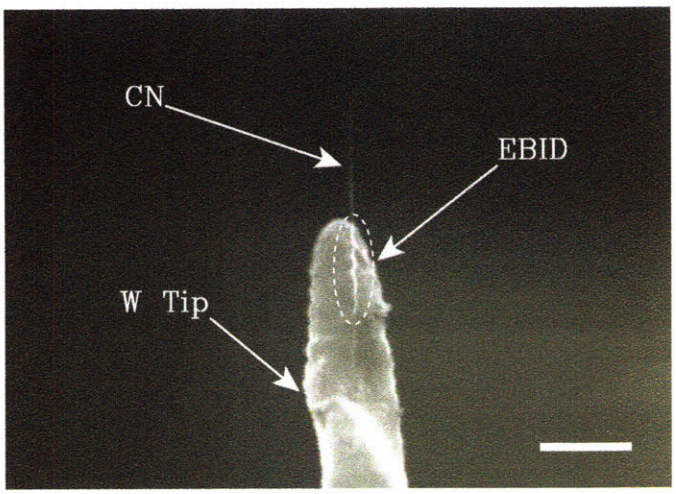


Figure 3-4: Scanning electron micrograph of a CN attached to a tungsten tip. The dotted circle represents the area which was magnified under the microscope to deposit the carbonaceous material. The scale bar corresponds to 2 μm.

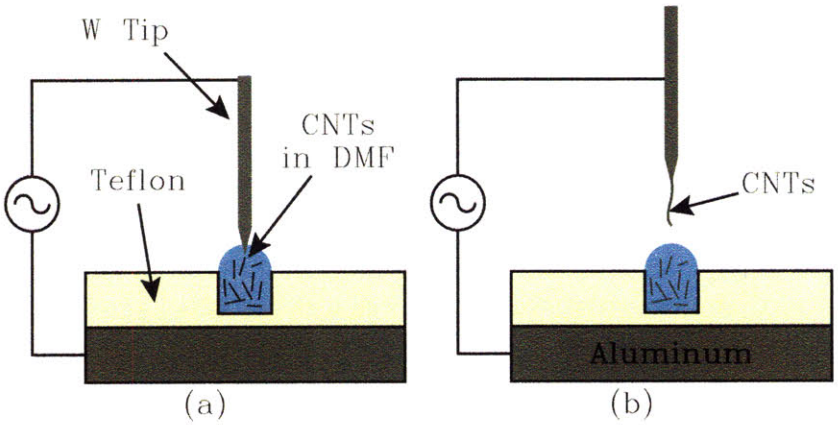


Figure 3-5: Schematic of the DEP setup (a) before and (b) after being drawn from a CNT solution.

min before the tip was retracted. A typical CNT bundle attached probe via DEP is shown in Figure 3-6.

3.1.3 Experimental Procedure

3.1.3.1 Two Terminal Measurements

In order to show the electrostatic actuation of a CN relay two probes are used in a "two terminal measurement" shown in Figure 3-7. In this measurement one probe has a CN attached by methods previously described and the second is a bare tungsten probe.

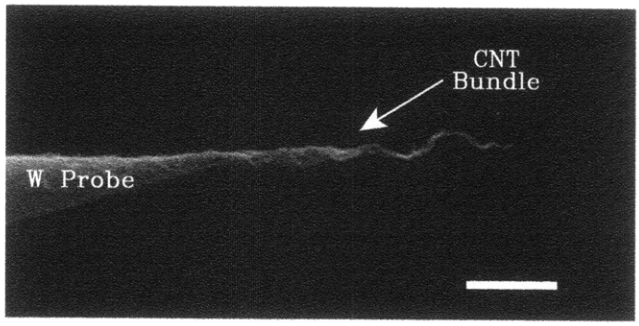


Figure 3-6: Scanning electron micrograph of a CNT bundle attached probe by DEP. The scale bar corresponds to 10 μm

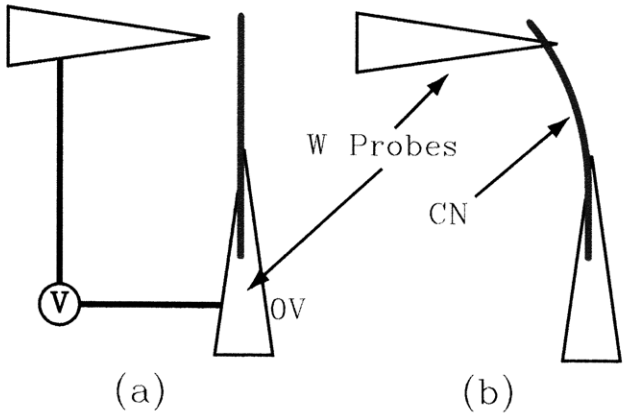


Figure 3-7: The setup of a two terminal measurement for pull-in. (a) The CN attached probe is grounded, and a voltage sweep is applied to the other probe. (b) As a result, the tube is pulled in to one side.

A voltage sweep is applied between the two probes, Figure 3-7a, the electrostatic force between the CN and the probe causes the CN to deflect and eventually make contact with the bare tungsten probe, Figure 3-7b. In a typical experiment, voltages are swept between 0 to 20V in increments of 0.01 to 0.05 V and current compliance is set to 20 nA. The current is limited via the current compliance in order to prevent the CN from burning out. The voltage at which the CN is pulled-in is assumed to be the voltage at which a sharp transition is observed in the current-voltage, I-V, sweep.

3.1.3.2 Three Terminal Measurements

In order to show pull-in and subsequent pull-off of a CN relay three probes are used in a "three terminal measurement" configuration shown in Figure 3-8 and is essentially an extension of the two terminal experiment. Initially, in stage 1 a CN attached

probe situated in the middle of two bare probes, Figure 3-8a, and a voltage sweep between the CN and one of the bare probe causes the CN to be is pulled into and eventually come into contact with the bare probe and a critical $V_{pull-in}$ and remains in contact, Figure 3-8b. Pull-off is demonstrated in stage 2, where a sweeping voltage is applied between the now in contact CN probe and the opposing bare probe, Figure 3-8c, when at a critical voltage $V_{pull-off}$ the CN is pulled-off one probe and comes into contact with the opposing probe, Figure 3-8d. Finally, the capability of this device is for multiple switching is demonstrated in stage 3, where another voltage sweep between the now in contact CN probe and the opposing bare probe, Figure 3-8e, causes the tube to be pulled-off yet again and come into contact the with opposing probe, Figure 3-8f. This second "pull-off" should occur at roughly the same $V_{pull-off}$ since the parameters of the tube such as length, diameter, and, most important, gap distance are equivalent in both cases.

3.1.4 Results

3.1.4.1 Two Terminal Measurements

Switching behavior was observed in multiple nanotubes tests by all attachment techniques. Figure 3-9 shows a scanning electron micrograph of a measurement conducted using a CN bundles attached via DEP. The corresponding I-V measurement is shown in Figure 3-10 for a bundle of nanotubes with a length of 100 μm, a cross sectional thickness of 200-300nm, and a gap distance of 30 μm. The individual nanotubes in the bundle had an outer diameter ranging from 25-50nm. From Figure 3-10 $V_{pull-in}$ is 3V.

3.1.4.2 Three Terminal Measurements

Figure 3-11 shows an example of a three terminal measurement. Initially a CN attached by van der Waals and EBID, shown in Figure 3-11b, was pulled to a right electrode, Figure 3-11b, and then pulled off onto a left electrode, Figure 3-11c, and then pulled off back onto the right electrode, Figure 3-11d. In these experiments pieces

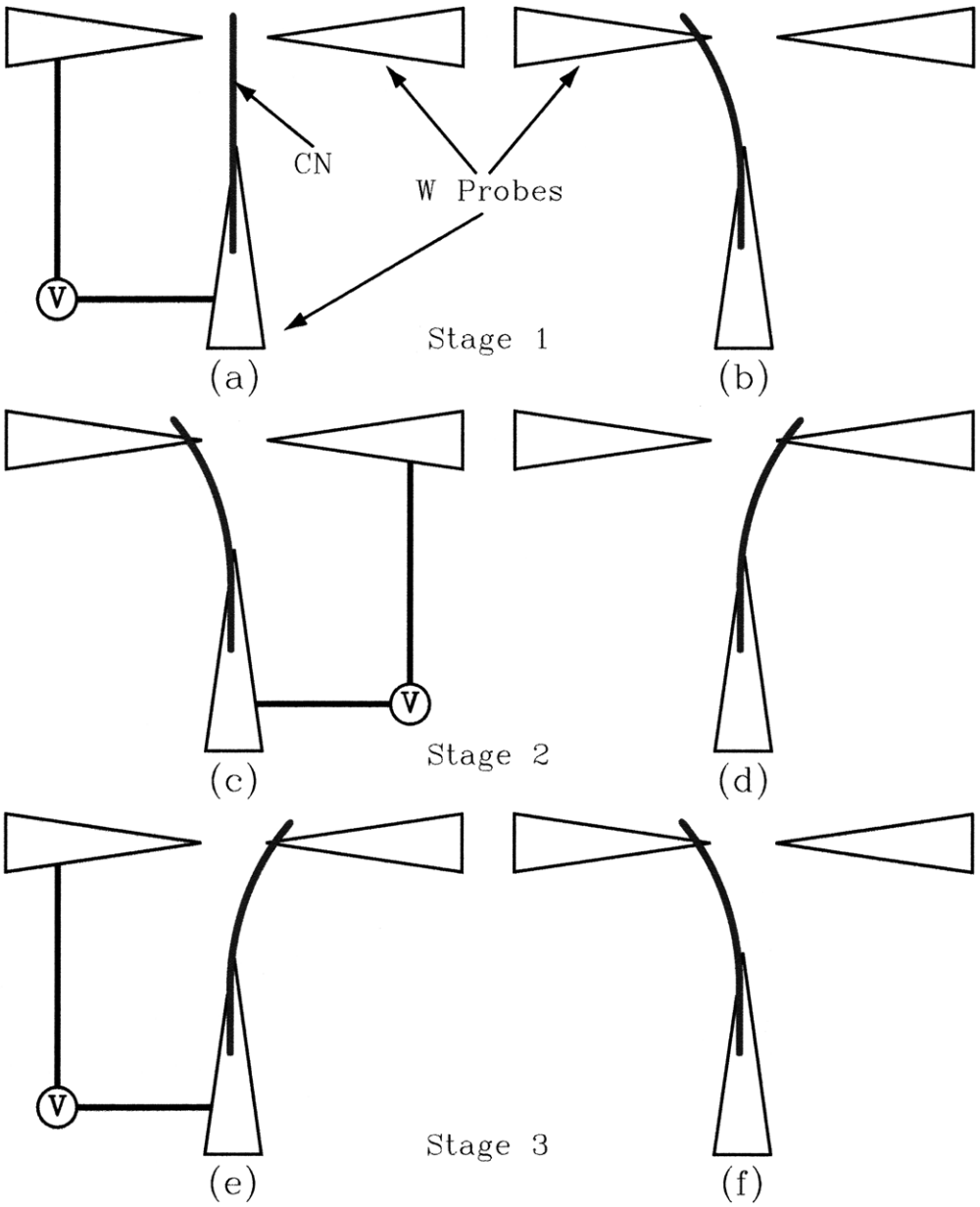


Figure 3-8: The setup of a three terminal measurement for pull-in and pull-off.

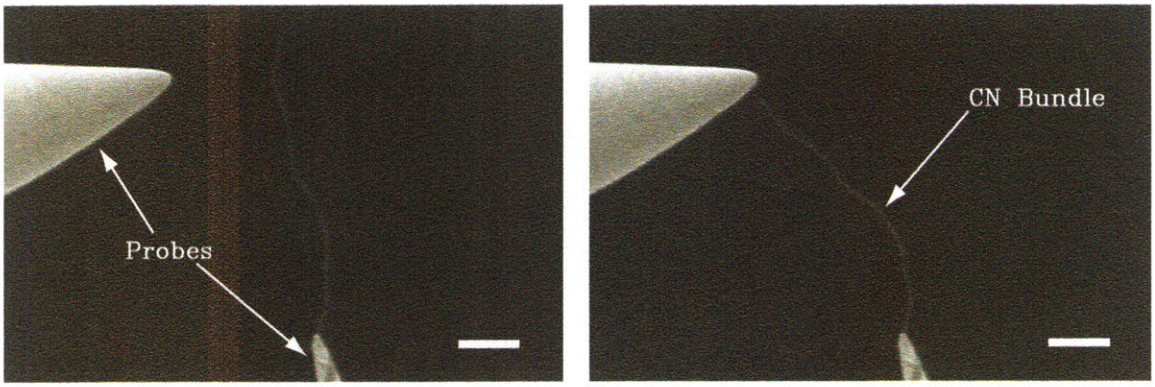


Figure 3-9: Scanning electron micrograph of a CN bundle a) before and b) after pull-in. The scale bar corresponds to 20 μm.

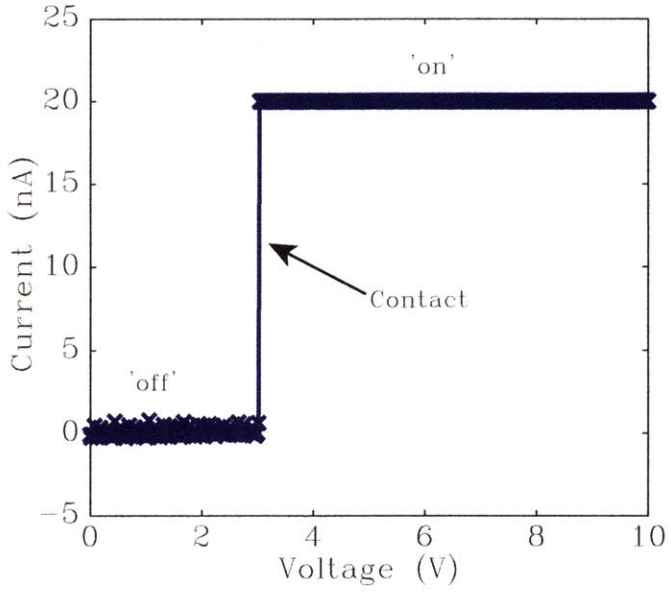


Figure 3-10: I-V measurement for a two terminal measurement. Corresponds to the scanning electron micrographs in Figure 3-9.

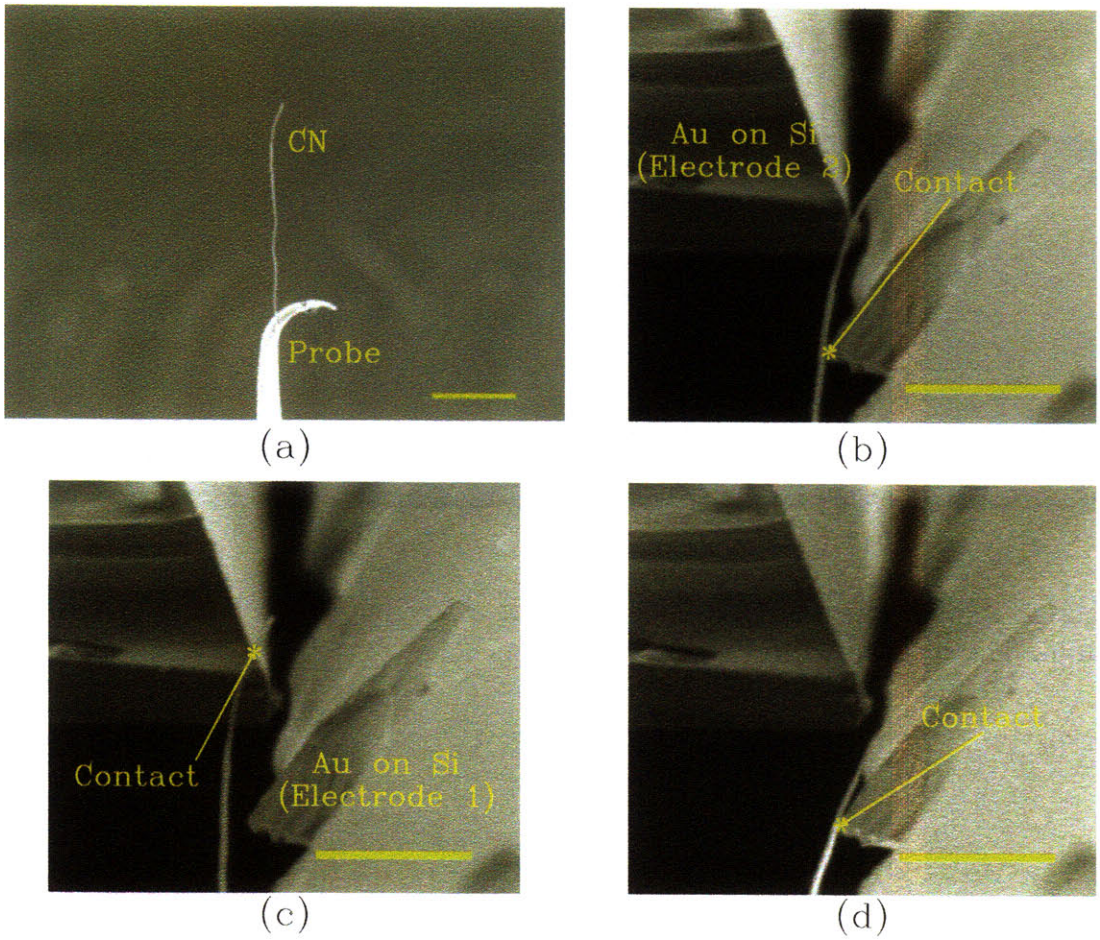


Figure 3-11: Scanning electron micrograph of a) CN attached probe. b) Same probe used in a three terminal measurement after step 1, c) step 2 and d) step 3. The scale bar corresponds to a) 20 μm and b,c,d) 10 μm.

of silicon with evaporated gold on chrome electrodes were used in place of tungsten probes. Since the SEM view shows a 2D image of the probe setup, using long pieces enabled easier alignment of the electrodes to the CN. Pull-in was demonstrated at a $V_{pull-in}$ of 5V and pull-off was demonstrated at a $V_{pull-off}$ of 20V. This was the first demonstration of a pull-off enabled three terminal switch and validation of devices operated by pull-off. The CN in this experiment had an outer diameter of 400nm and a length of 55μm, and the initial gap between the tube and the electrode was 1μm.

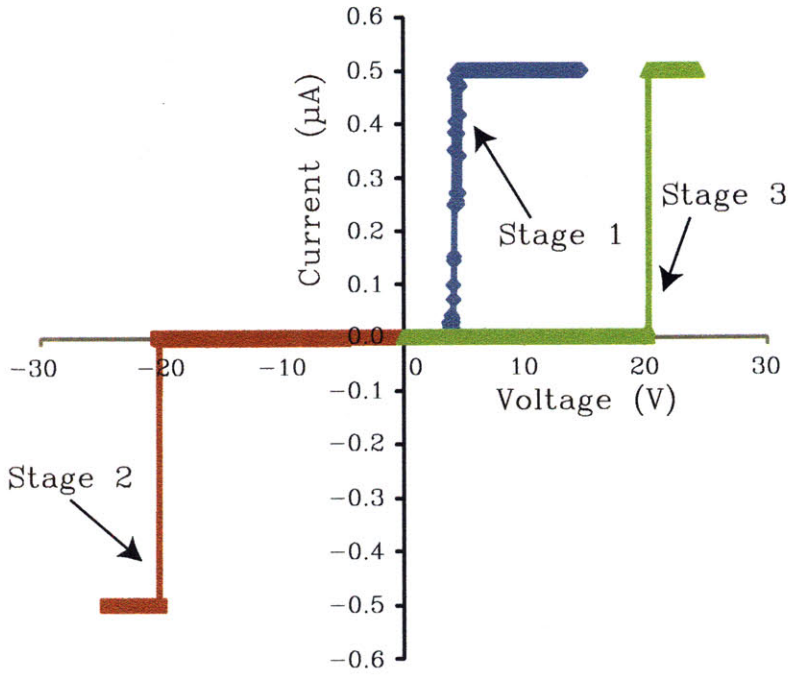


Figure 3-12: I-V measurement for a three terminal measurement. Corresponds to the scanning electron micrographs in Figure 3-11.

3.2 Initial design

In this section a first generation fabrication scheme is presented. Initially it was expected that this fabrication scheme would be used for a fully integrated device but was later used for further prototyping by introducing a CN with the nanopositioner rather than growing the CN from the device directly. The initial fabrication scheme was based on the following design requirements: 1) high aspect ratios and 2) contacts that are well aligned to CNs.

3.3 Fabrication

The initial fabrication scheme is shown in Figure 3-13. In this fabrication scheme a well aligned gap is created by defining the gap as well as the tube growth location in a single mask step in order misalignments associated with multiples masking steps.

The process begins with a P-type, boron doped, .001-005 Ω-cm silicon with a 100nm of thermally grown oxide substrate, Figure 3-13a. A dog bone shaped beam

consisting of 100nm thick Au on a 10nm Cr adhesion layer, which will later be broken up to act as two independent electrodes, is photolithographically patterned by liftoff, Figure 3-13b. A 250nm thick layer of 950k PMMA is spun on the sample and functions as both etch mask and lift-off layer in subsequent steps, Figure 3-13c. A 100nm line is exposed and developed in the PMMA, Figure 3-13d. Transene gold and chromium etchant are used to etch the metal layers not masked by the PMMA, the metal layers are over etched to create an eventually undercut to define a gap between the CN and the contacts, Figure 3-13e. Buffered oxide etch is used to removed SiO_2 not covered by the PMMA and the metal layers, Figure 3-13f. The final etch is performed with XeF_2 to create a large aspect ratio pit in the silicon layer without etching the mask, Figure 3-13g. A 20nm nickel layer is then evaporated by electron beam evaporation and lifted off, Figure 3-13h. This is as far as the fabrication was performed, but the final structure was meant to be realized when the entire structure is placed in a specially designed PECVD furnace for the growth of CNs from a catalyst, Figure 3-13i. The actually growth of CNs by this method are discussed in the next chapter. The final device is shown in Figure 3-13j.

Images at various stages of the fabrication are shown in Figure 3-14, and the final device with an evaporated nickel catalyst is shown in Figure 3-15.

Even though this fabrication technique was never fully used to realize an integrated CN device, the materials used in this fabrication were tested designed to withstand the high temperatures processes in the growth of CNs. Figure 9-2 is an atomic force micrograph of the gold contacts showing little to no sign of dewetting of the gold before and after an anneal of 900C for 1 hr, this lack of dewetting was facilitated by the chrome diffusion/adhesion barrier used in the process. Nonetheless, the process itself is a novel technique for creating high aspect ratio self-aligned structures.

3.4 Issues

Although the prototyping and initial fabrication provided key proof-of-concept information towards realizing a vertically oriented carbon nano-relay several limitations

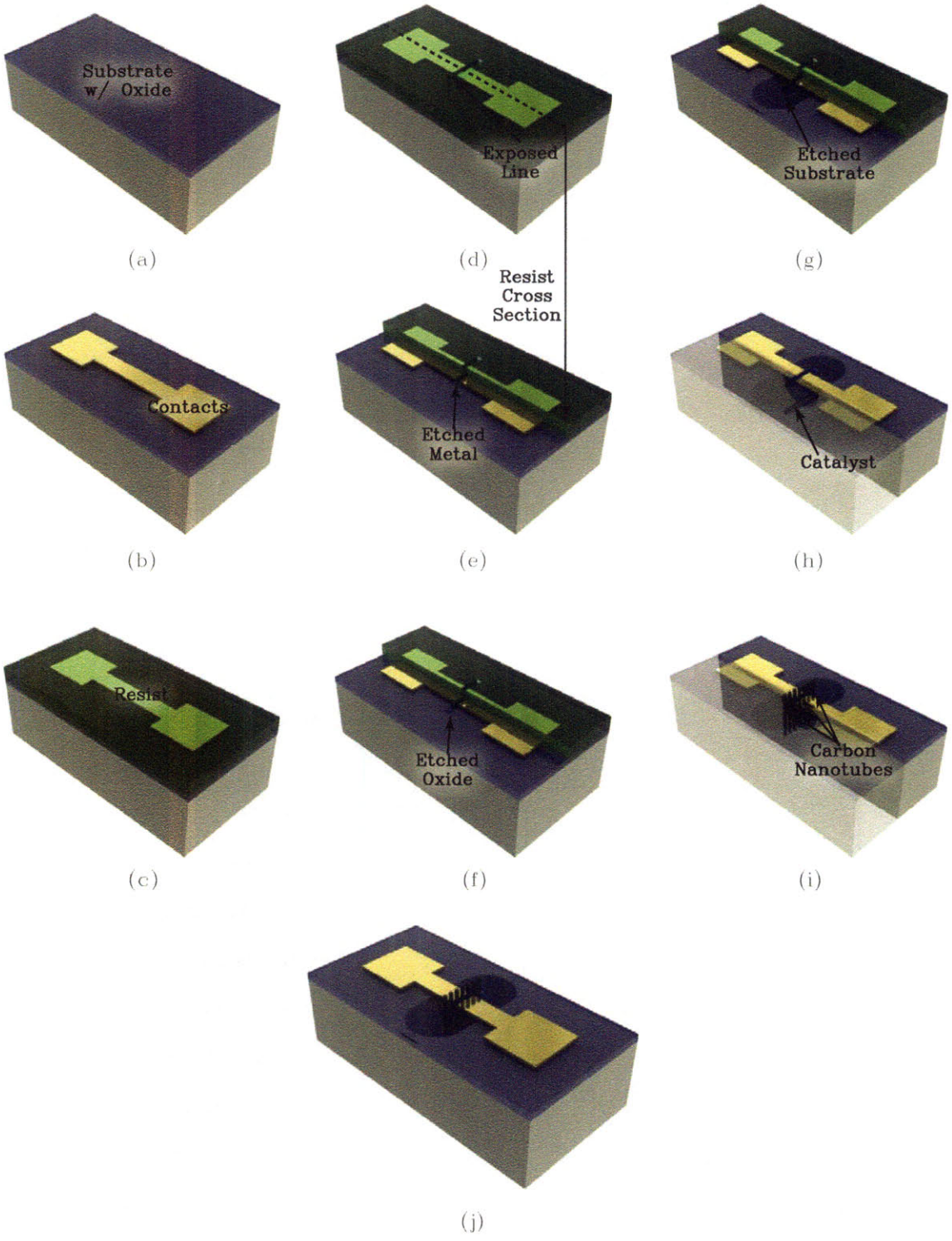


Figure 3-13: Initial fabrication route for integration and prototyping. Schematic of various stages of fabrication: a) substrate with thermal oxide, b) photolithographically patterned gold contacts, c) coating of the electron beam resist, d) exposed and developed trench pattern in resist, e) resist masked etching of the metal contact, f) resist masked etching of the oxide, g) resist masked etching of the silicon, h) deposition and lift-off of the metal catalyst, i) growth of the tube, and j) the final device.

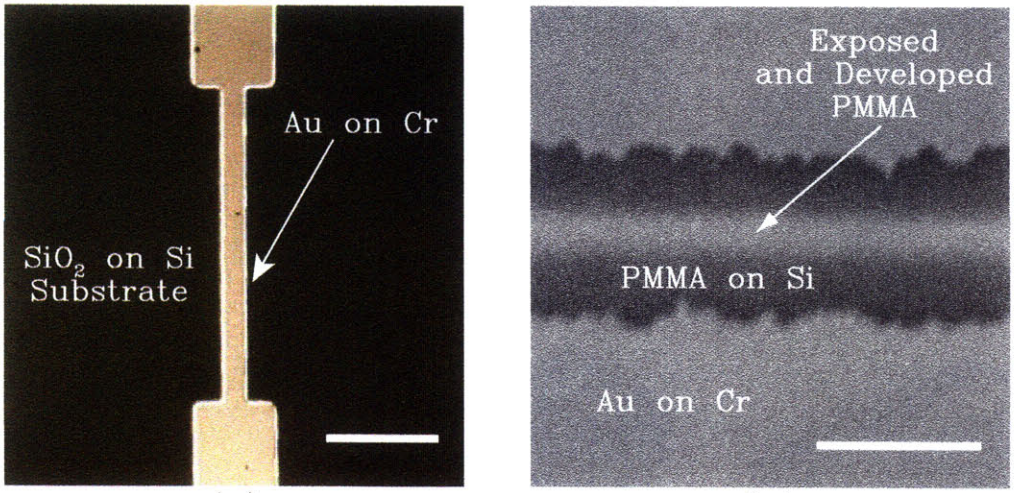


Figure 3-14: Micrographs of initial fabrication efforts. a) Photomicrograph of a Au on Cr beam schematically shown in Figure 3-13b. b) Scanning electron micrograph of the gap defined via a PMMA mask after the oxide etch schematically shown in Figure 3-13f. The scale bars correspond to a) 100 μm and b) 1 μm.

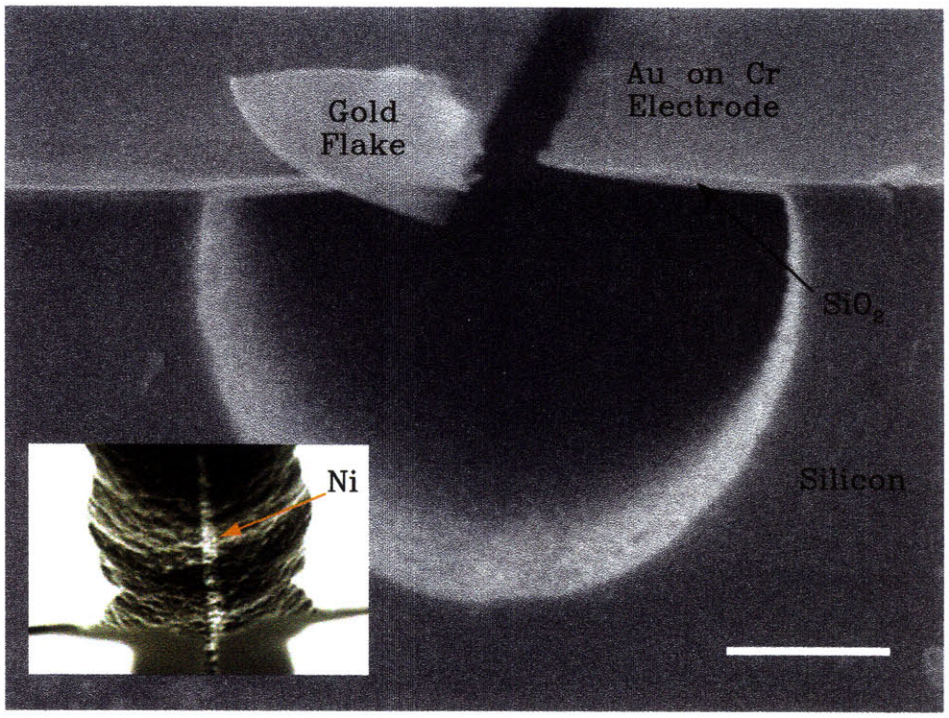


Figure 3-15: Cross section scanning electron micrograph of the initial fabrication efforts after the liftoff of the catalyst schematically shown in Figure 3-13i. The inset is a high contrast tilted scanning electron micrograph of the channel showing the 100nm Ni wide catalyst line . The scale bars correspond to 2 μm.

prevented comprehensive studies by these means. Reproducible results were very difficult to obtain for a variety of reasons. One reason was the limitations in the alignment of probes to electrodes resulted in inconsistent gap sizes. This was primarily as a result of doing a 3-dimensional alignment between the CNs and the electrodes, while only having a 2-dimensional spacial view under the SEM. This also created a problem when measuring the contact area between the CN and the electrode, be they tungsten probes or sections of gold on silicon. The other major issue was a result of variations in the CNs used in these experiments. As discussed in the Chapter 2, mechanical properties of CNs can range widely depending on a variety of factor, least of all being CNs from different sources. CNs attached to probes were in general highly prone to failure, so a single CN attached probe could not be continuously used tested in order to validate the continuum models proposed in Chapter 2. An example of this is shown in Figure 3-16 which was a test using a CN attached bundle via DEP dropped into a trench that was fabricated by the methods described in the previous section. Figure 3-16a is a scanning electron micrograph before the tube was pulled into the right contact and Figure 3-16b is an image after the bundle was pulled-in and then immediately exploded. The failure mechanism can be understood from the equivalent circuit in Figure 3-17. During pull-in, the tube bundle and pull-in contact form plates of a capacitor, C_{ES}. On contact this capacitor discharges and the large current can destroy the bundle. A series resistor, R_S, cannot be used to minimize the discharge current. Rather, it is necessary to either increase the contact resistance, R_C, or lower the pull-in voltage, $V_{pull-in}$. This difficulty was further enhanced by the time consuming, serial nature of the measurement, since only a single device could be measured at a time. Again, this section served more as a validation for the concept of creating a device with pull-off than anything else.

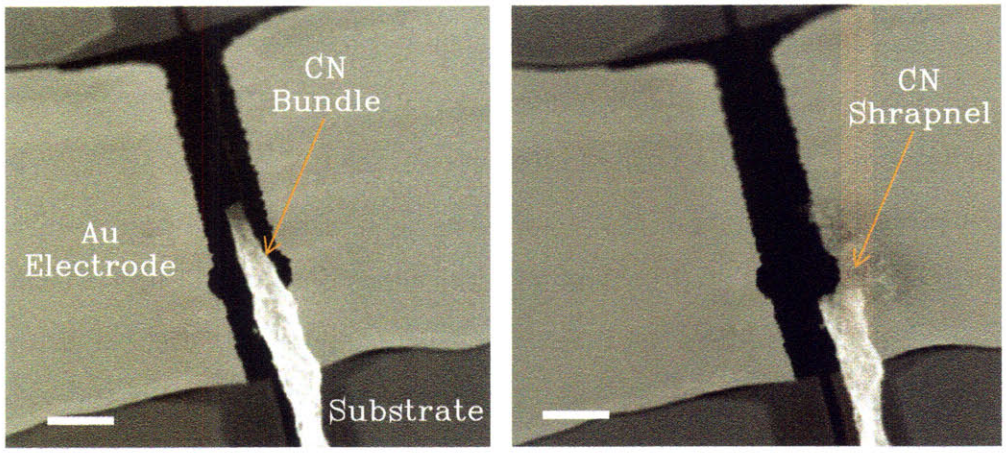


Figure 3-16: Scanning electron micrographs of a CN attached bundle via DEP, a) before and b) after testing. The scale bars correspond to 2 μm.

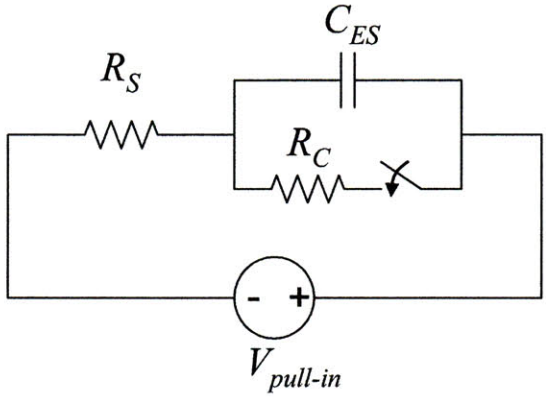


Figure 3-17: The equivalent circuit of the NEM. On contact the switch closes and the capacitor discharges. The discharge current can destroy the tube bundle.

Chapter 4

Integration

4.1 Need for integration

One of the most obvious advantages of a wafer integrated device is parallel processing for creating and testing devices. In addition, integration of a vertically oriented carbon nano-relay offers several unique advantages. In the previous chapter comprehensive studies were limited by reproducibility of both the CNs used as well as the gap size. Wafer scale integration solves both of these problems. Rather than rely on randomly extracted CNs, CN heights and dimensions can be controlled by varying growth conditions discussed in Section 4.2.1. Also self-aligned tailored gap sizes can be set by the thickness of a grown insulator discussed in Section 4.2.2. Furthermore, large current spikes due to low resistance contacts was the primary cause of CN destruction in previous proof-of-concept experiments, Figure 3-16, and can be avoided and controlled via variable resistance doped silicon electrodes discussed in 4.2.3

4.2 Fabrication

The overall fabrication scheme is based on a self-aligned photoresist planarization technique first developed by Chen et al for the fabrication of double-gated vertically aligned carbon nanofiber field emitter arrays. [8] The process begins with the growth of a carbon nanotube grown on TiN substrate from a Ni catalyst, Figure 4-1a, and is

followed by the deposition of a conformal layer of PECVD deposited silicon dioxide (SiO_2) and doped amorphous silicon (a-Si), where the oxide acts as an insulator and the doped a-Si functions as the gate contact. A self-aligned photoresist planarization technique is executed by spinning a layer of resist on the wafer such that thickness of the resist is less than that of the of the CNT/SiO_2/a-Si, Figure 4-1b. This process automatically planarizes the surface and allows the gates to be opened without etching the rest of the wafer without any sort of lithographic alignment. The resist is then removed, Figure 4-1c, and a buffered oxide etchant is used to remove the oxide and finalize the device, Figure 4-1d.

Since the process uses the combination of a vertically oriented structure with aligned contacts, the use of a similar process towards the fabrication of a vertically oriented carbon nanotube based relay was a good fit. Thus, there were several modification implemented to the process for use with relays: 1) The use of a line of tubes rather than an individual tubes, 2) the self-aligned photoresist planarization technique was changed to a self-aligned planarization and thin technique, and 3) the addition of a step to split the conformally coated a-Si gates contact into two isolated contacts.

The fabrication is as follows, and is shown in Figure 4-2. The device consists of a row of MWCNTs grown with contacts grown on either side of the row with an air gap separating the MWCNTs from the contacts as shown in Fig. 1. In order to create the row of MWCNTs, 5μm rows consisting of 200nm diameter dots with a 400nm pitch were patterned by e-beam lithography on a highly doped Si substrate (Figure 4-2a) with a sputtered 50nm TiN diffusion barrier layer (Figure 4-2c). A 30nm thick layer of Ni was then deposited using e-beam evaporation at a vacuum of $< 10^{-6}$ torr and lifted-off to define the catalyst for CNT growth (Figure 4-2c). All the growths were performed in a 6" Black Magic Pro PECVD system from Aixtron and incorporates a direct current plasma-enhanced chemical vapor deposition (dc-PECVD) chamber with a high temperature substrate heater to facilitate the growth of CNTs using a standard recipe for the growth of isolated carbon nanotubes. The growth was performed by initially pumping the system chamber to 150 mtorr. A flow of Ar gas

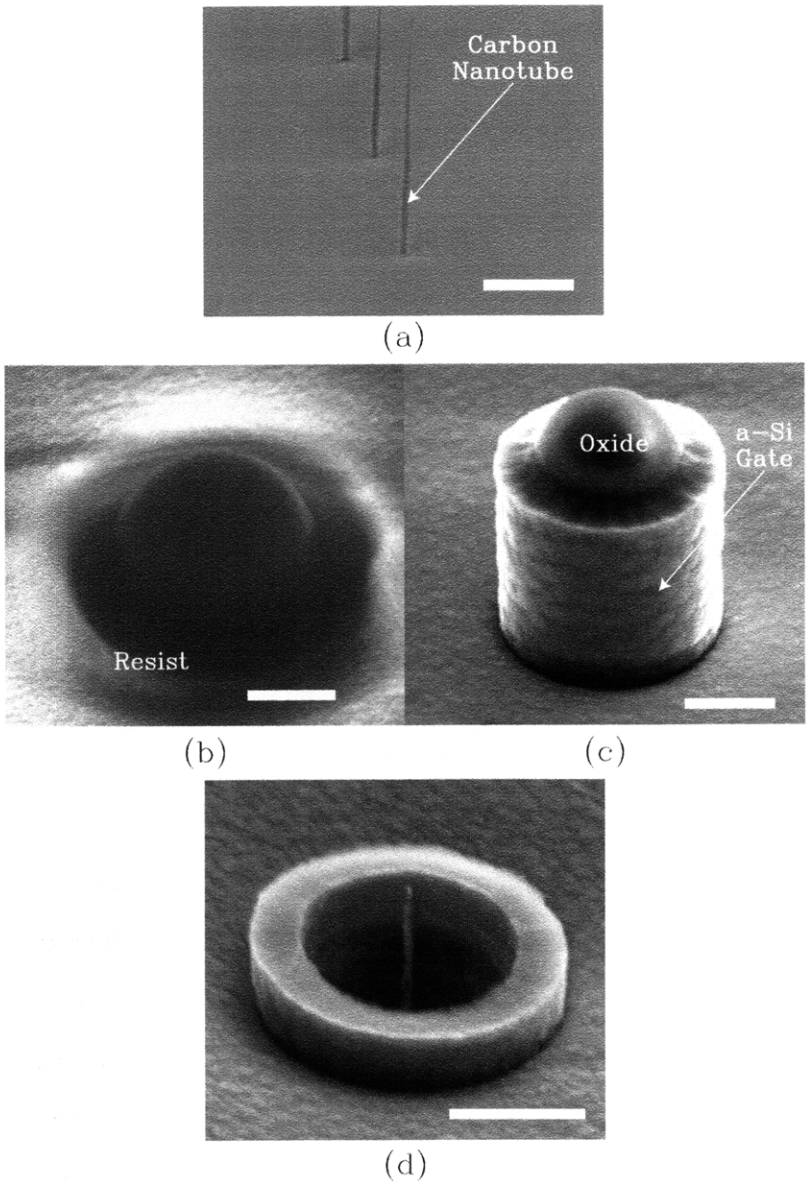


Figure 4-1: Fabrication carbon nanotube based gated field emitter. The scanning electron micrographs show various stages of the fabrication: a) the growth of carbon nanotube, b) the top of the emitter poking out of the resist after the use of a self-aligned photoresist planarization technique, c) the same device after an a-Si etch and removal of the photoresist, and d) the final device.

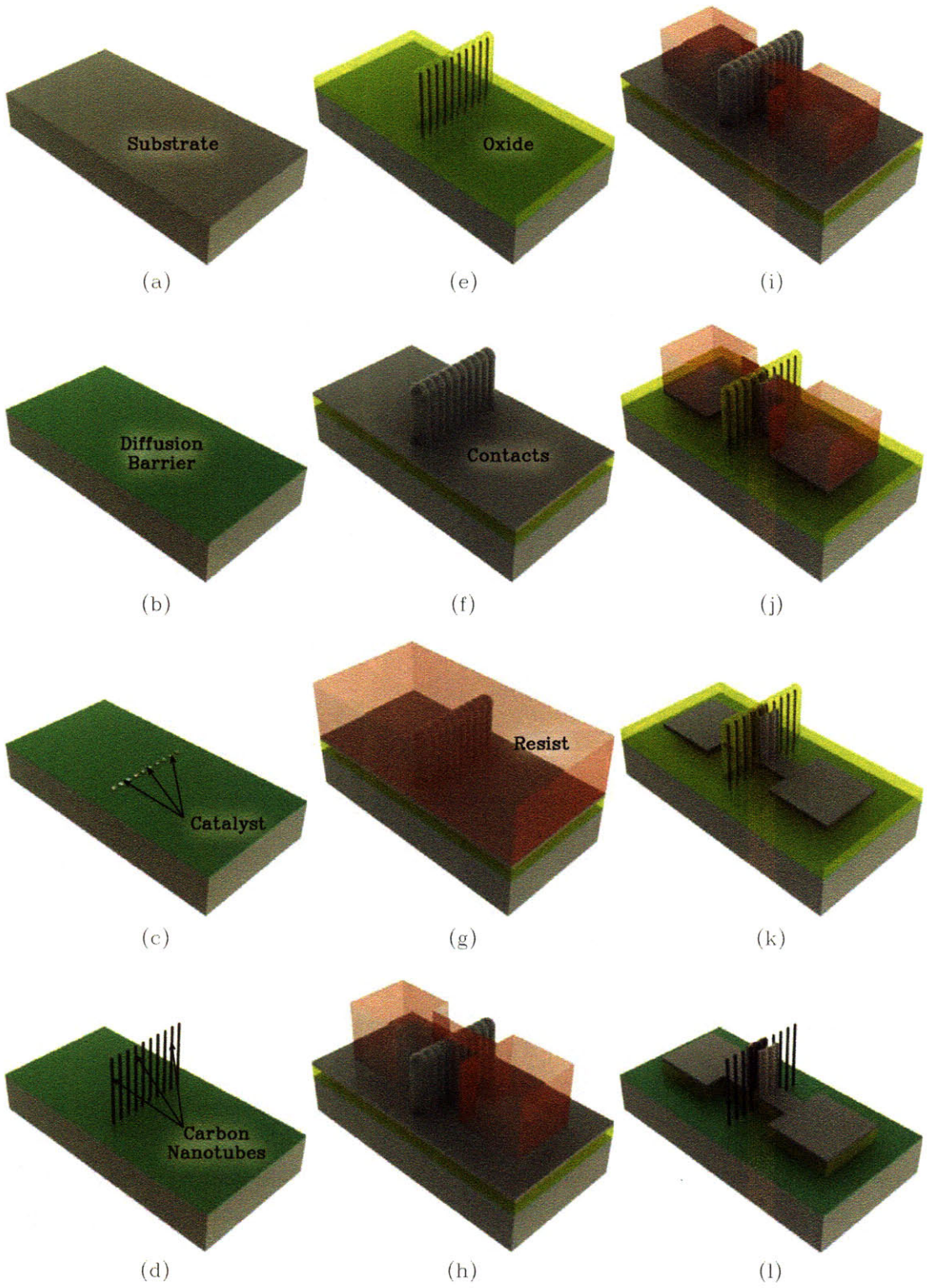


Figure 4-2: Schematic of fabrication process for a fully wafer integrated vertical carbon nano-relay: a) Bare silicon wafer, b) sputter deposited TiN layer, c) lift-off patterned catalyst sites, d) CN grown, e) PECVD oxide deposition, f) PECVD a-Si deposition, g) spun resist, h) patterned resist, i) etched resist, j) etched a-Si, k) ashed resist, and l) final released structure.

was introduced into the chamber and the substrate was heated to a temperature of 825C. A mixture of C_2H_2 and NH_3 was introduced and a plasma power of 120W was applied to the substrate for a growth time of 30 min, Figure 4-2c. An SiO_2 insulation layer was deposited using PECVD to conformal coat around the tubes, Figure 4-2e, and was followed by an in-situ P-doped a-Si deposition, Figure 4-2f. A layer of resist of about 10μm was spun such that the tops of the tubes (about 500nm-1μm) were above the resist (Figure 4-2g). A series of 200μm squares pads separated by a 100μm gap and bridged by a 5μm line were patterned, so that the line was perpendicular and coincident with the row of tubes (Figure 4-2h). The resist was then thin with a combination of resist over-developing and oxygen plasma etching, or "ashing," to expose the tops of the row of CNT/SiO_2/a-Si pillars (Figure 4-2i). The resist layer acted as a mask for the a-Si contact pads as well as the aligned electrodes, which were patterned by using an electron cyclotron resonance (ECR), reactive ion etch (RIE) (Figure 4-2j). The samples were again ashed, this time to completely remove the resist mask (Figure 4-2k) and then wet etched with buffered oxide etchant and cortical pointed dried to create the final structure (Figure 4-2l). The specific details of the fabrication are addressed in the rest of this section.

4.2.1 CN Growth

Although there are several techniques generally used in the synthesis of carbon nanotubes and nanofibers, including thermal [38] and plasma enhanced [58] chemical vapor deposition, laser ablation [22], and arc discharge [26], our requirements limit that selection. In examining the design for the switch, we require individual tubes or individual lines of multiwalled nanotubes that are vertically oriented with relatively large aspect ratios. Based on these set of criteria the only suitable method of growing carbon nanotubes for our application is plasma enhanced chemical vapor deposition (PECVD).

4.2.1.1 CN PECVD Primer

PECVD growth of carbon nanotubes was first demonstrated by Ren et al. [58] First a transition metal catalyst, i.e. Ni, Fe, or Co, from which the carbon nanotubes are grown, are deposited onto a substrate. The catalyst is either deposited across a large area to create "forests" of nanotubes or can be patterned to form an isolated nanotube at a specific location. Selection of the catalyst type and thickness is significant in that it can dictacte many of the attributes, for example the diameter, growth rate, height, etc., of the nanotubes that are grown. A brief survey of catalyst selection will be covered in covered in Section 4.2.1.2. Often times a diffusion barrier such as TiN is deposited prior to the catalyst, in order to prevent the diffusion of catalyst such as nickel in to silicon. [55]

The carbon nanotubes are grown in a modified PECVD system schematically shown in Figure 4-3. The substrate is heated to temperatures ranging from 600-900°C at a low pressure under a flow of ammonia (NH_3)gas. The ammonia functions to pretreat the catalyst in order to form seed sites and activate the catalyst for CNT growths as the substrate heats up, this stage will be referred to as the "pretreatment" stage. During this pretreatment stage, the plasma can be sparked in order to further assist in the activation of the catalyst. If not sparked during the pretreatment stage, the plasma can be sparked during the "growth" stage, where a gas mixture containing a carbon source gas and diluting gas, typically acetylene and ammonia, is then introduced into the system to initiate the growth of carbon nanotubes. The diluting gas, ammonia, also functions to etch amorphous carbon (a-C) from being deposited and sustaining the growth of the nanotubes. [63] The plasma itself serves two purposes during the growth stage. The first is to, in addition to thermal cracking at the sample surface, assist in cracking the carbon source and etch gases. Once the carbon source is cracked, carbon is available to dissolve into the catalyst, where upon reaching some saturation level in the catalyst, precipitates to form carbon nanotubes. During this process of diffusing and precipitating, the carbon nanotubes can either grow via a base growth mechanism or a tip growh mechanism, both of which are illustrated in

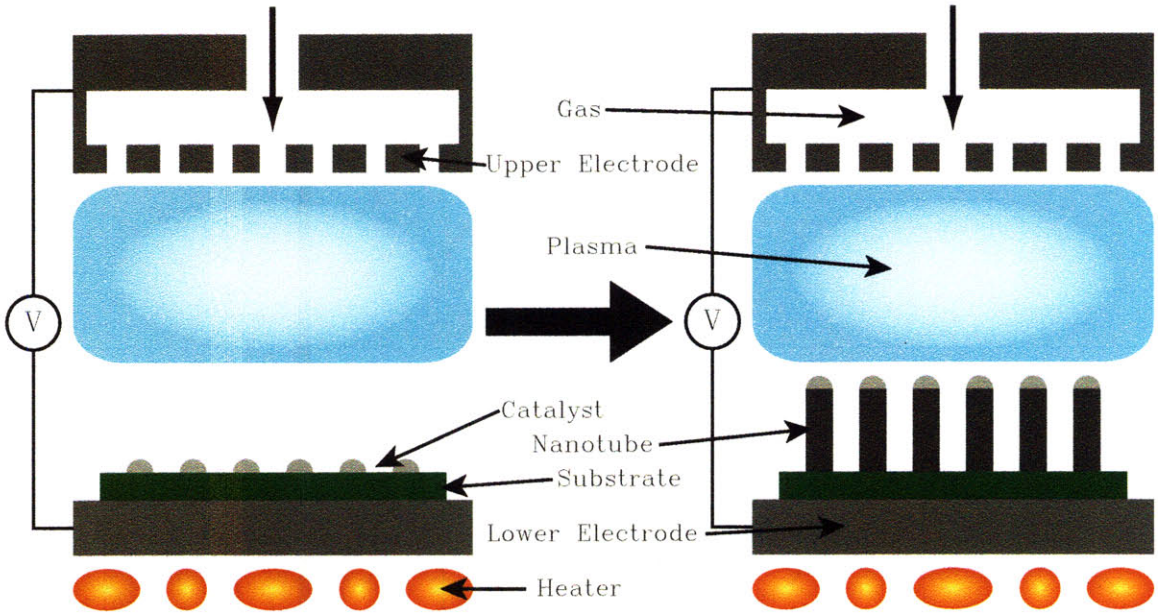


Figure 4-3: Schematic of PECVD reactor and synthesis of vertically oriented carbon nanotubes. The PECVD reactor for nanotube growth is similar to a standard PECVD reactor in that it consists of a vacuum chamber in which we have two electrically isolated electrodes. A growth gas in then introduced into the chamber, a plasma is sparked, and material is then deposited in the system. The primary difference is the the bottom electrode, on which the substrate sits, is in close proximity to a high temperature heater. High temperatures are necessary to "activate" the catalyst for nanotube growth. In addition, as opposed to a conventional PECVD where the material is deposited everywhere, growth only occurs underneath the catayst.

figure 4-4. In the case of PECVD grown nanotubes, tip growth is the most dominant and is shown in figure 4-5, where a forest of carbon nanotubes were grown from a nickel source and imaged before and after being etched with a nickel etchant. The second purpose of the plasma is to vertically aligned the carbon nanotubes due to the presence of a large electric field in the plasma sheath. [6]

4.2.1.2 Catalyst Selection

As stated in section 4.2.1.1, CNs can be grown from a variety of transition metal catalyst. For comparison several transition metals: nickel (Ni), cobalt (Co), and Iron (Fe), were investigated as potential catalysts for CN growth. The comparison was conducted using 10 nm films of each metal on highly doped Si substrates with a 50 nm TiN diffusion barrier. Carbon nanotube forest were grown instead of isolated

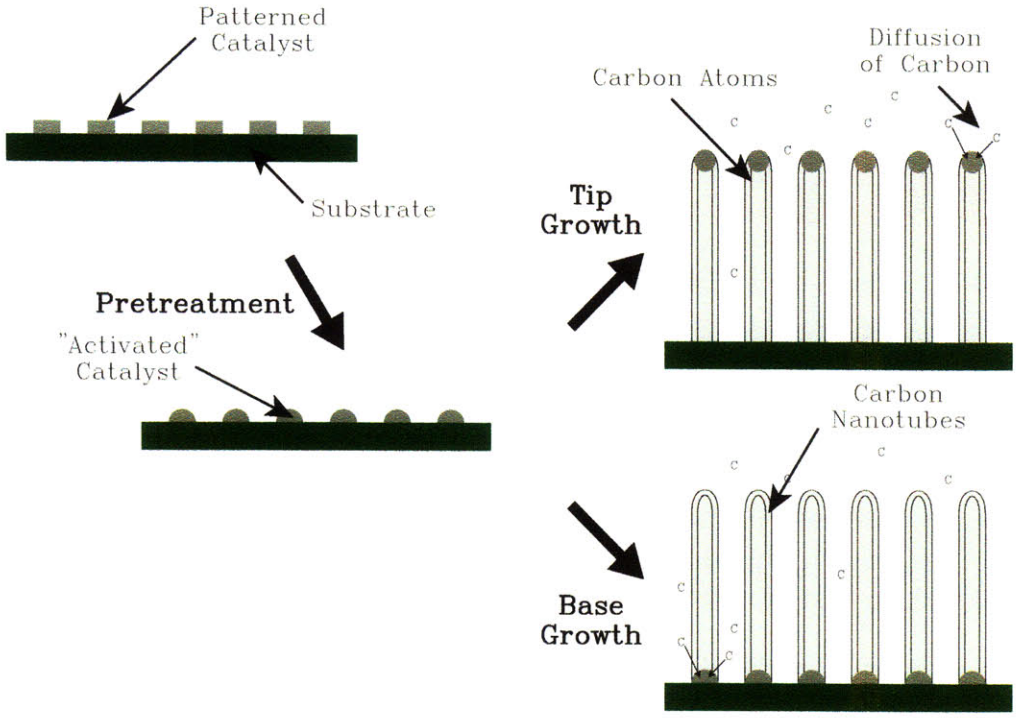
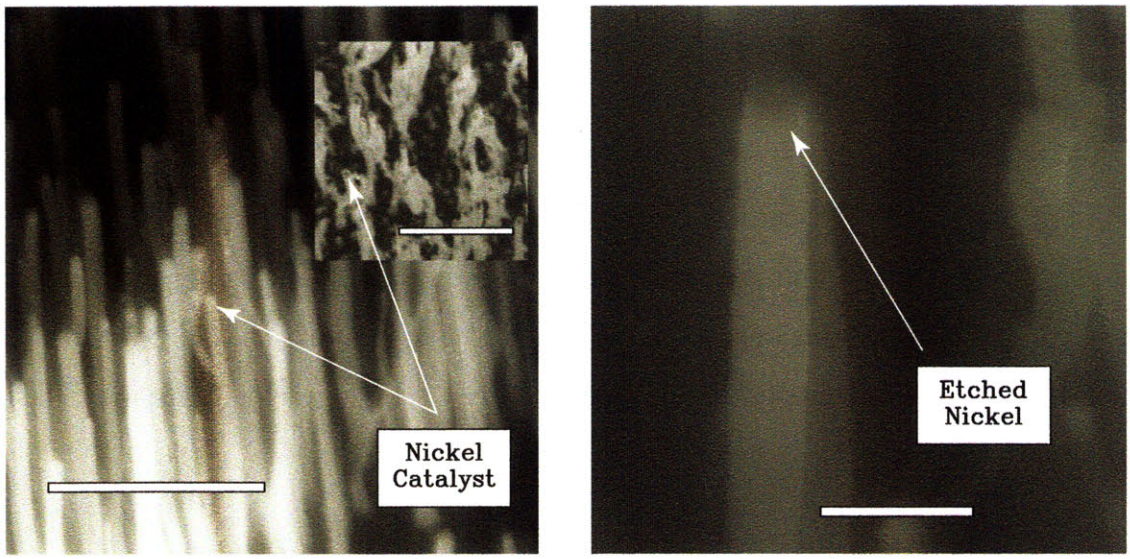


Figure 4-4: Schematic drawing of the growth cycle of carbon nanotubes derived from patterned catalyst. Initially the catalyst and substrate are pretreated, typically involving heating of the substrate under some sort of inert or reducing environment. Growth begins when carbon is introduced, and diffused into the catalyst. The carbon nanotubes can then grow by either having the carbon precipitate out from the top of the catalyst resulting in a base growth or from the bottom of the catalyst resulting in a tip growth.



(a) (b)

Figure 4-5: Scanning electron micrographs of a nanotube forest showing evidence of a tip based growth mechanism. a) Shows the image of the forest as grown, the inset is of the edge of the sample and shows an alternative contrast the bright and dark spots, respectively show the location of the nickel catalyst. The scale bar corresponds with 1μm b) Shows the same image after the sample was placed in nickel etchant. The arrow points to the location where the catalyst was removed. The scale bar corresponds to 200nm. Samples were grown from a 10 nm Ni film on a 50 TiN on silicon substrate.

Catalyst	Ht Avg (μm)	Ht StdDev (μm)	Tip Dia Avg (nm)	Tip Dia StdDev (nm)
Iron	1.1	0.25	50	10
Cobalt	1.6	0.97	70	20
Nickel	1.9	0.26	85	15

Table 4.1: Comparison of several catalysts based on the average nanotube height and tip diameter as well as distributions of both parameters.

tubes for convenience. All comparisons are based on forests that were grown at the same time, Figure 4-6, and were judged on several figures of merit relevant to the final device, including tube height, uniformity, and tube size. From the results shown in Table 4.1 nickel was selected. Although nickel exhibited the largest tip diameter resulting in a larger pull-in voltage according to Equation 2.19, it's large height more than compensates for this due to the the faster decrease in pull-in voltage with height than increase with diameter. In addition, the prior use of nickel as a catalyst makes it the logical choice. [8]

4.2.1.3 Growth Limitation

From Equation 2.19, in order to achieve the lowest possible switching voltage it is of critical importance to create devices where the length of the CNTs are as large as possible. In this section some of the limitations of nanotube growth are examined. Early growth results suggested that the limit in height of the CNTs are in large part due to the initial volume of the catalyst. Several experiments were conducted to determine the effects of catalyst volume on the height of isolated carbon nanotubes as well as the cause of volume limited growth of carbon nanotubes.

In order to determine effect of catalyst volume on CNT growth, samples with varying catalyst volume were created. Initially, variations in catalyst volume were created by varying the catalyst area while keeping the thickness equal. The catalyst pads were patterned to less than 400 nm in order to ensure the nucleation of a single carbon nanotube. [64] For these set of experiments, a 10 nm thick e-beam deposited nickel catalyst was deposited on a highly doped Si substrate with a sputtered 50nm

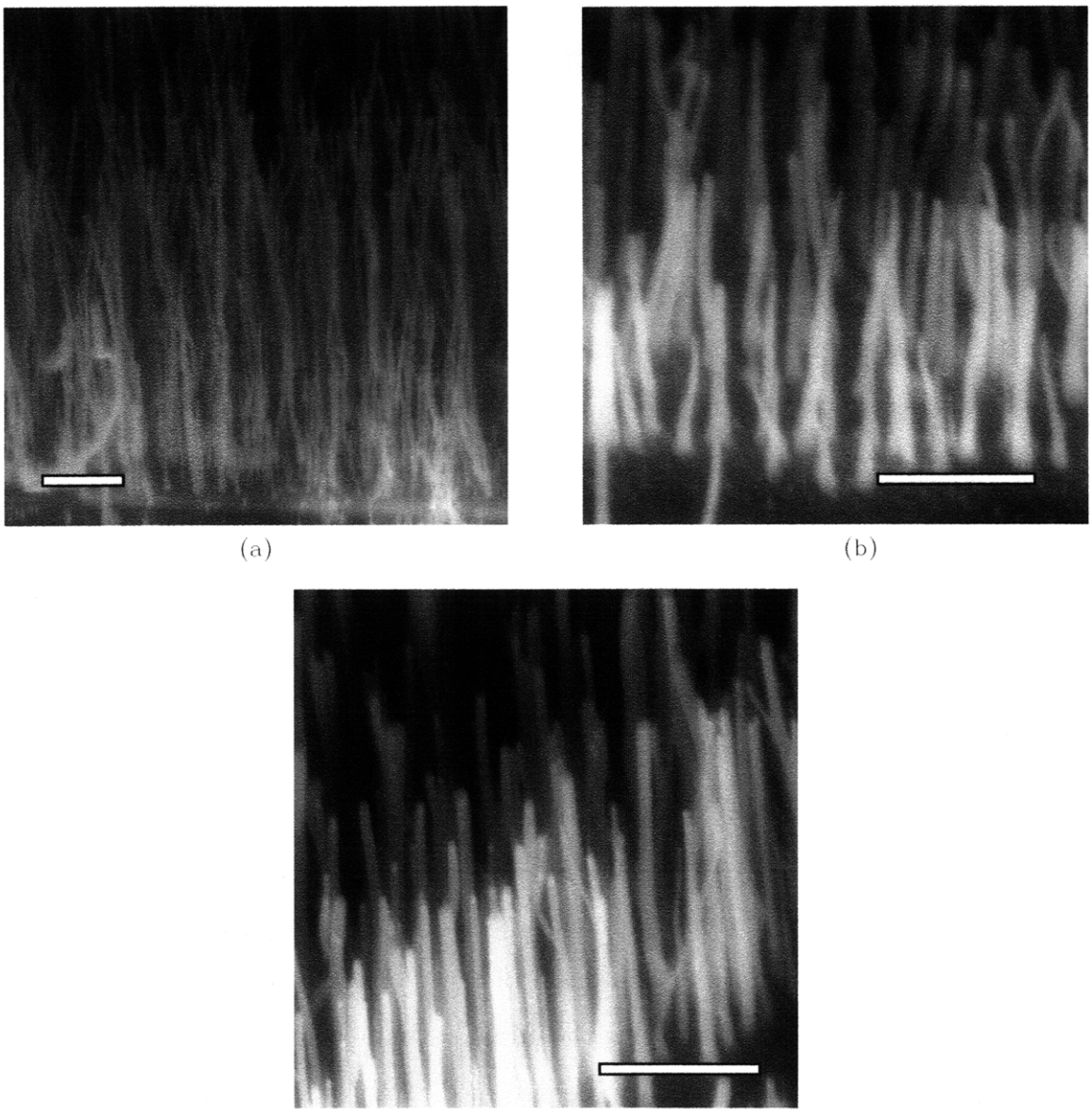


Figure 4-6: Scanning electron micrographs of carbon nanotube forests grown from a) cobalt, b) iron, and c) nickel. All three samples were grown under the same conditions at the same time.

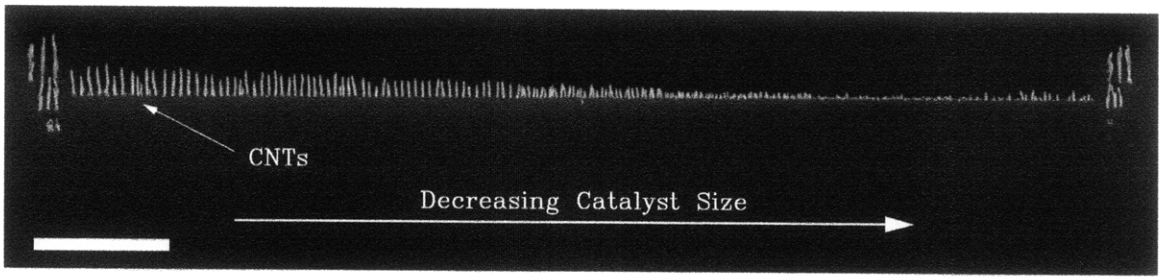


Figure 4-7: Scanning electron micrographs of a line of carbon nanotubes. Line shows how the height of the nanotubes decreases with decreasing catalyst volume. Catalyst sizes decrease by 50nm every 11μm. The scale bar corresponds to 10 μm.

TiN diffusion barrier layer. Catalyst pads ranging from 70-320 nm in increments of 50 nm were patterned via e-beam lithography and lift-off method. The carbon nanotubes were grown at 825C for 30 min under a 1:4 mixture C_2H_2 and NH_3. Upon heating, samples were annealed under NH_3, once the growth temperature was achieved C_2H_2 was introduced and a 120W plasma was sparked. Figure 4-7 shows the resulting CNT growth.

From Figure 4-9, it is apparent the size of the catalyst does not have that much of an influence of the diameter of the tube. This is true except except for the smallest patterned catalyst size, where there is, in general, little or no tube growth so it can be considered insignificant. Since the bottom tube diameter is independent of the patterned catalyst, the difference in nanotube height versus patterned catalyst size in figure 4-10 is concluded to be as a result of variations in catalyst volume. This is again illustrated in figure 4-8, showing the initial patterned catalyst and the resulting nanotube growth. The question left to be answered is why is nanotube growth limited by the volume of the catalyst?

As we grow tubes, catalyst is sputtered off, i.e. the same carbon and hydrogen atoms responsible for growing the nanotubes and etching the amorphous carbon, respectively, are being accelerated towards the substrate due to the electric field in the plasma, colliding, and subsequently removing nickel from the substrate, Figure 4-11. This is also by no means a new concept, in fact Merkulov et al at the ORNL speculated that catalyst sputtering during growth was the root cause of tip sharpening

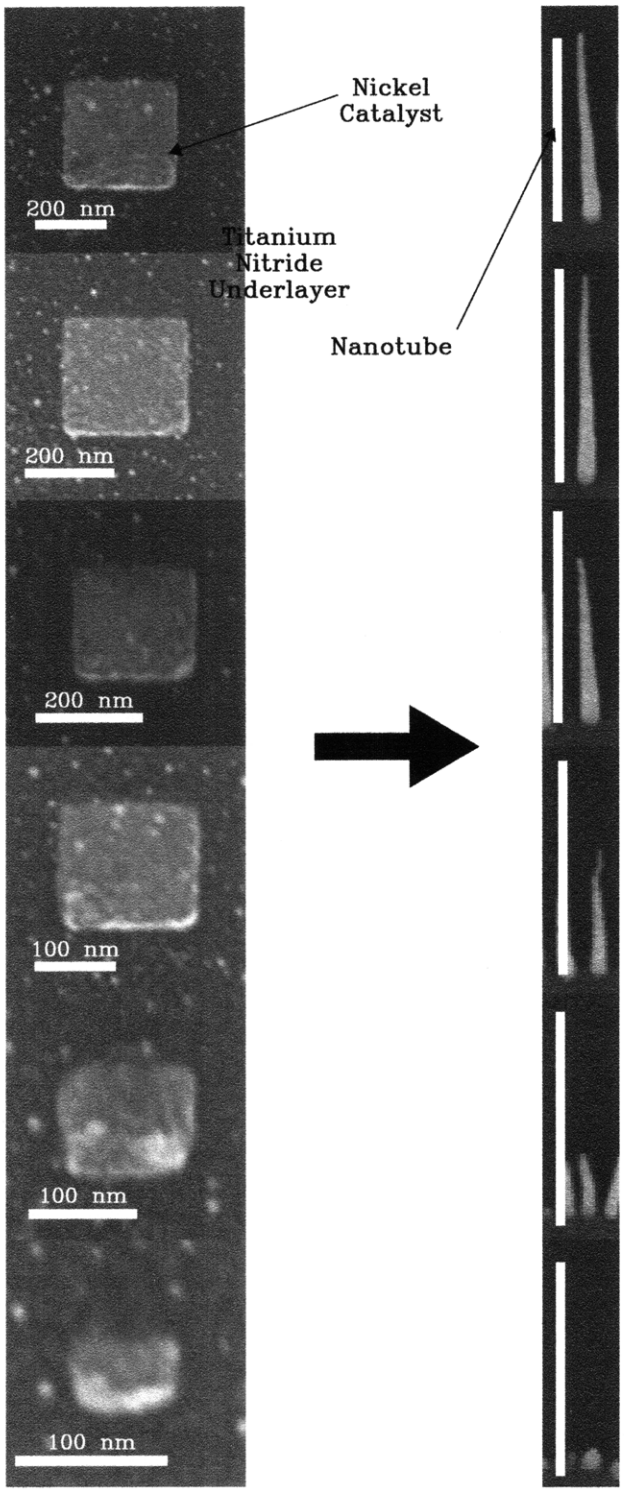


Figure 4-8: Scanning electron micrographs of a pre-patterned catalysts of varying size and their corresponding carbon nanotubes. Non-labeled scale bars corresponds to 1 μm.

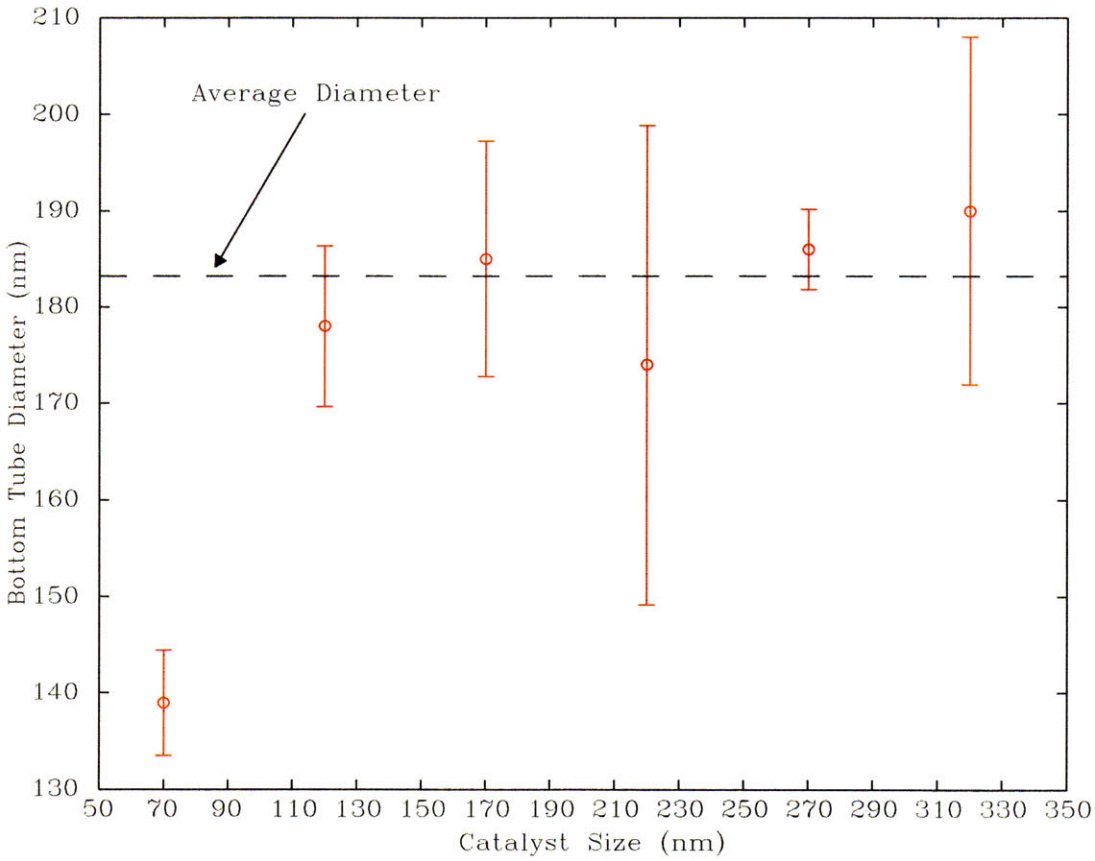


Figure 4-9: Plot of the catalyst size versus bottom carbon nanotube diameter. All measurements were taken from the same sample during a single growth.

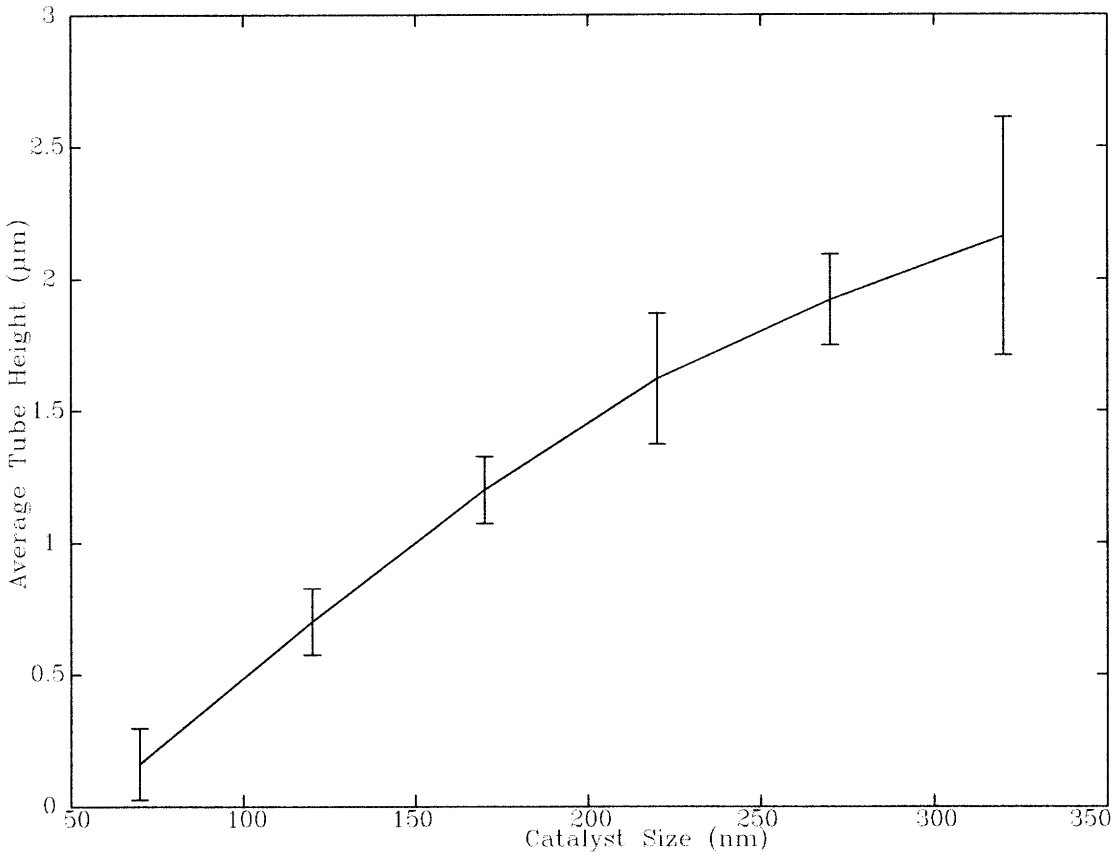


Figure 4-10: Plot of the catalyst size versus carbon nanotube height. All measurements were taken from the same sample during a single growth.

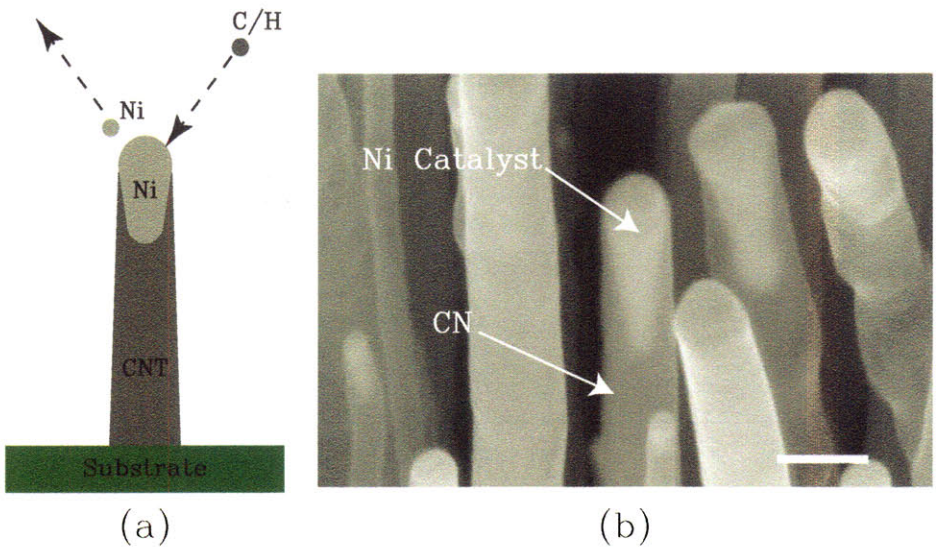


Figure 4-11: a) Schematic of nickel sputter off. b) Scanning electron micrograph of nickel catalyst at the tips of the nanotubes that are being sputtered off. The scale bar corresponds to 200 nm.

in their vertically aligned carbon nanocones, [50] but the work presented provides more experimental evidence to support this conclusion than that previously reported. In order to prove the concept of catalyst sputtering, an experiment was conducted in which several substrates with equivalent nickel thickness were grown with the same exact recipes except for the amount of time during which the plasma was turned on during the pre-treatment phase of the growth. Given the fact that for a decreased nickel thickness there is a decrease in tube height, Figure 4-12, again implying that less catalyst correlates to shorter tubes; if an increase in plasma anneal time during pretreatment corresponds to a decrease in tube height, than that implies that the initial volume of catalyst was decreased by sputtering of the nickel due to the plasma. This is precisely what is observed in Table 4.2 with the decrease in tube height with increase in plasma anneal time, providing strong evidence for sputtering limited catalyst growth.

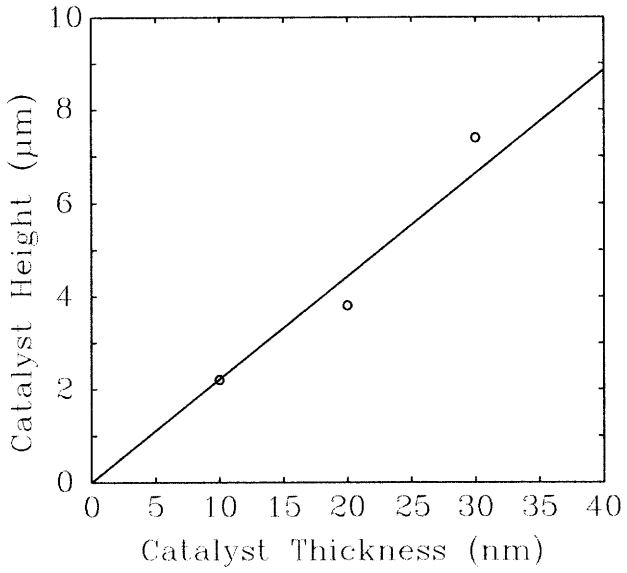


Figure 4-12: Plot of the catalyst thickness versus carbon nanotube height.

Ni Thickness	**Plasma Anneal**	**Avg Height**	**Std Dev**
30 nm	2-3 min	7.4 μm	1.3 μm
30 nm	60 sec	8.7 μm	1.1 μm
30 nm	30 sec	9.2 μm	1.3 μm

Table 4.2: Varying plasma anneal time while keeping nickel thickness constant.

4.2.2 Oxide Deposition

The next step in the fabrication is the growth a conformal oxide via PECVD using N_2O, N_2, and SiH_4 as the deposition gases. The exact processing conditions are outlined in the appendix. Just as a note, the oxides were grown with a chuck and shower temperature of 200°C to facilitate the growth of a doped amorphous contact in the next step.

As was previously stated, the CN aspect ratio plays a large role in the performance of the device, but from Equation 2.19 the distance between the CN and the contact, g, has an almost equal contribution towards achieving low voltage pull-in. This section will primarily focus on the limits of creating small gap structures. Figure 4-13 illustrates how the minimum achievable gap size, g_{min}, depends on the thickness of the grown, t_{ox} of the oxide, the minimum size which is dictated by the pitch, p of the carbon nanotubes by:

$$g_{\min} = \frac{p}{2}$$

The ideal $g_{ideal,\min}$ is grown to be a factor of safety of 1.5x above the $g_{\min}$ in order to avoid gaps between the CNs. Gaps between the tubes are detrimental in that they can lead to shorts in the final device, Figures 4-15 and 4-16.

Unfortunately, the growth of oxide via PECVD is not conformal as in the ideal case, Figure 4-14. The actual growth of oxide can be quite asymmetric. Figure 4-17 illustrates the fact that the deposition rate between the CNs, $rg_{ox,fill}$, is slower than the general gap defining oxide growth rate, $rg_{ox,gap}$. For the early stages of oxide growth, an example of which is a device with an undergrowth of oxide seen in Figure 4-16, $rg_{ox,fill} \sim rg_{ox,gap}$ but as the oxide gets thickers and the spacing between the gaps gets smaller so does $rg_{ox,fill}$. A similar effect is seen when PECVD oxide is employed to fill trenches and usually results in void formation. In these structures void formation is attributed to lack of surface migration of the reactants leading to an angular dependent growth. [48] The result of this is an oxide growth rate that s greater on the top of the trench than the bottom, eventually pinching off the top

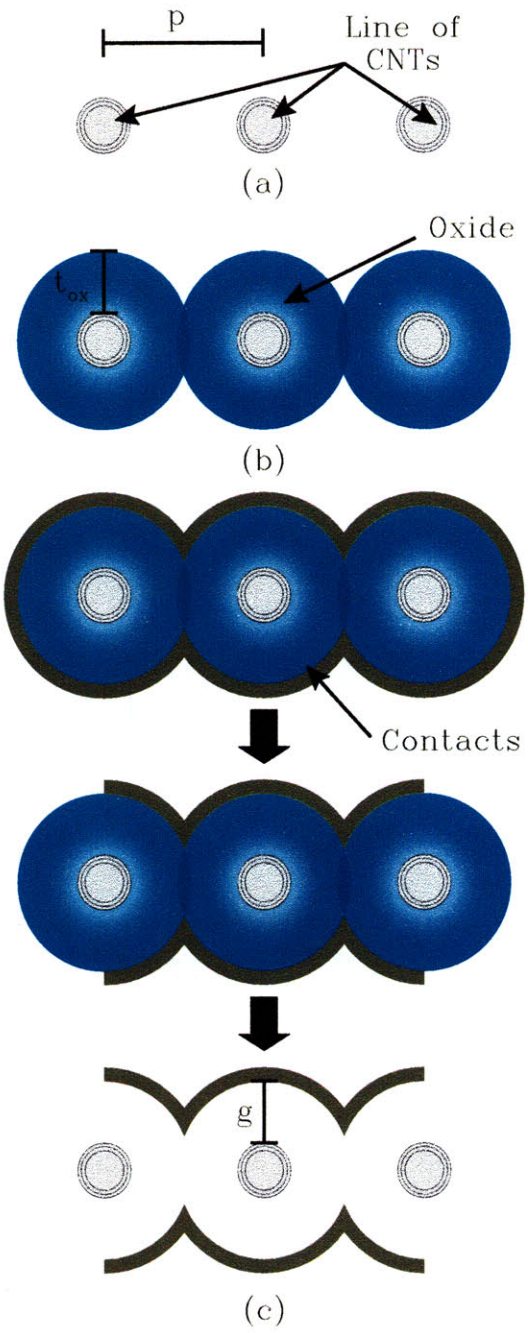


Figure 4-13: Schematic of the fabrication of the device after tube growth a) starting with a line of CNs, grown with a pitch, p, b) growth of a PECVD oxide with thickness, t_{ox} and c) the deposition of the contacts and final processing.

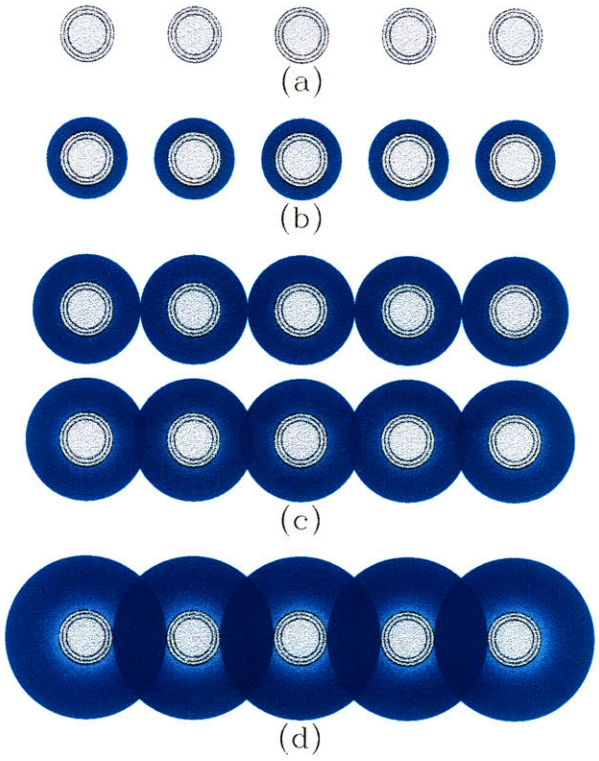


Figure 4-14: Schematic of the ideal growth of a conformal oxide with showing a) the original line of CNs, b) the undergrowth of oxide, b) (upper) the minimum thickness of oxide required optimal growth and (lower) the optimal growth of oxide with given factor of safety, and d) an undesired overgrowth of oxide.

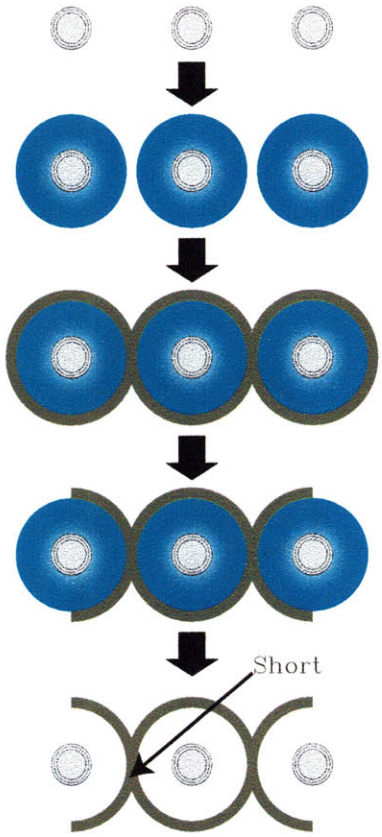


Figure 4-15: Schematic of the fabrication of the device in which the oxide between tubes did not coalesce leading to a short between the two electrodes.

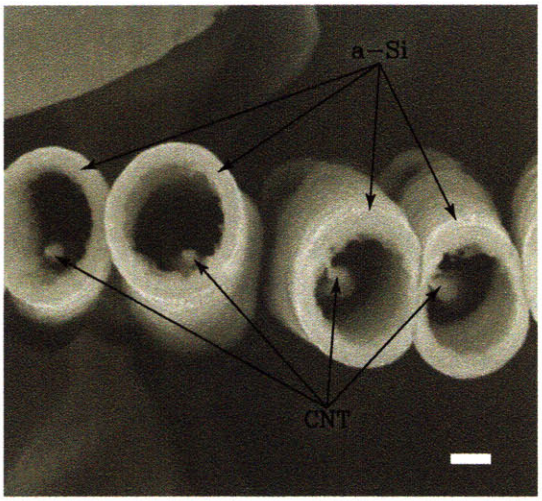


Figure 4-16: Scanning electron micrograph of a device with an undergrowth of oxide. The scale bar corresponds to 200nm.

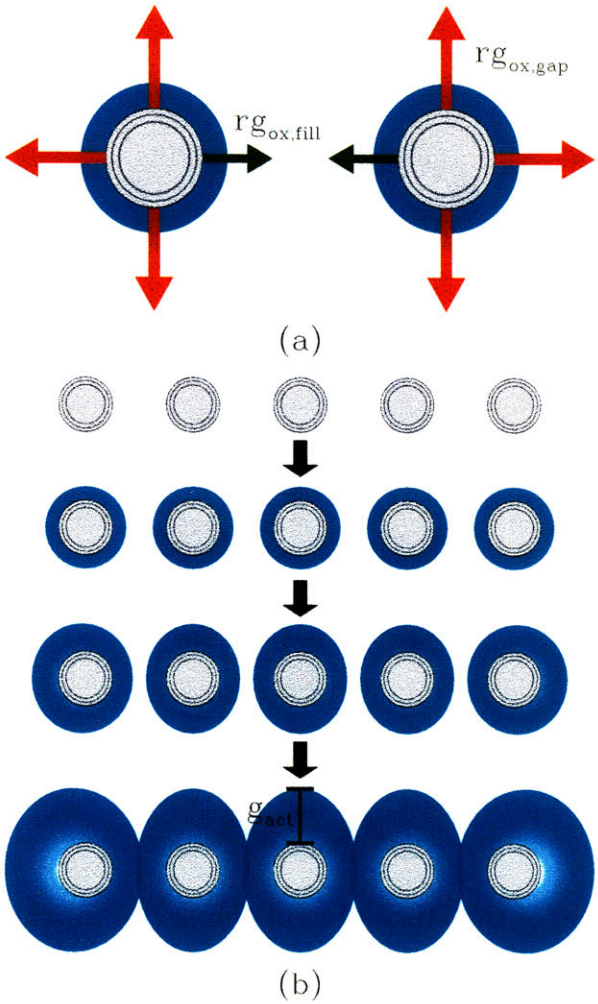


Figure 4-17: Schematic showing a) two different growth rates the first being the faster, uniform rate of oxide growth, $rg_{ox,gap}$ and the second being the slower rate of oxide growth, $rg_{ox,fill}$, between the tubes and b)the resulting growth of this asymmetric growth rate

of the trench and creating a void. This explains some of the gap formation since a mushroom style growth would also form voids on the bottom. This does not however explain the asymmetric oxide growth shown in Figure 4-17, the result of which are an oval shaped oxide around the nanotubes shown in Figure 4-18

It is suspected that the difference in $rg_{ox,gap}$ and $rg_{ox,fill}$ is primarily due to charges trapped in the film during PECVD deposition of films. [70] The charges themselves are embedded more or less isotropically, but as the the gap fills the growth rate is slower in the region between the CNs. In this region the gap is small enough that the

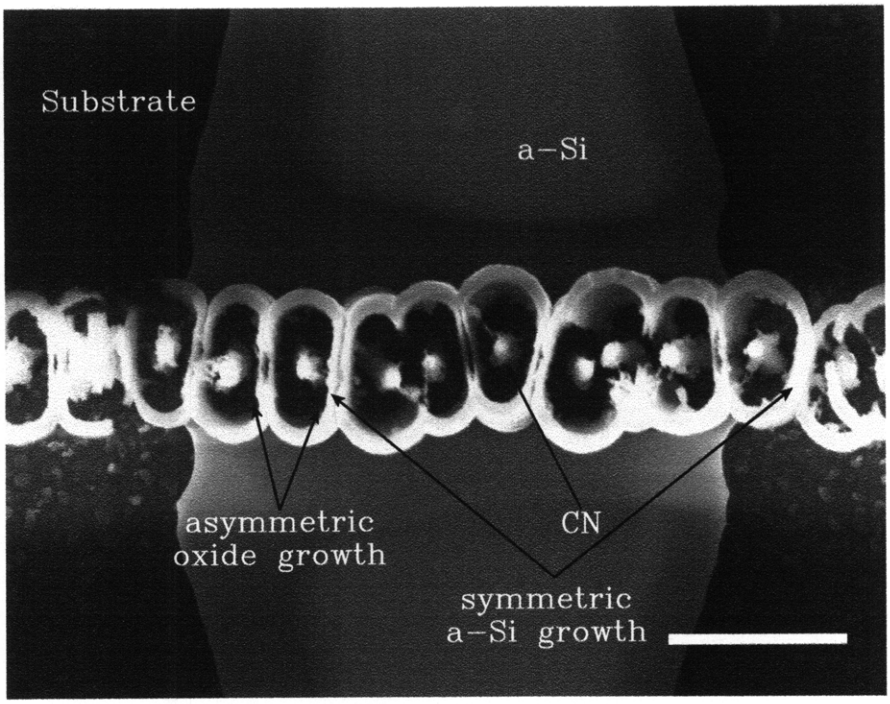


Figure 4-18: Schematic of the ideal growth of a conformal oxide with showing a) the original line of CNs, b) the undergrowth of oxide, b) (upper) the minimum thickness of oxide required optimal growth and (lower) the optimal growth of oxide with given factor of safety, and d) an undesired overgrowth of oxide.

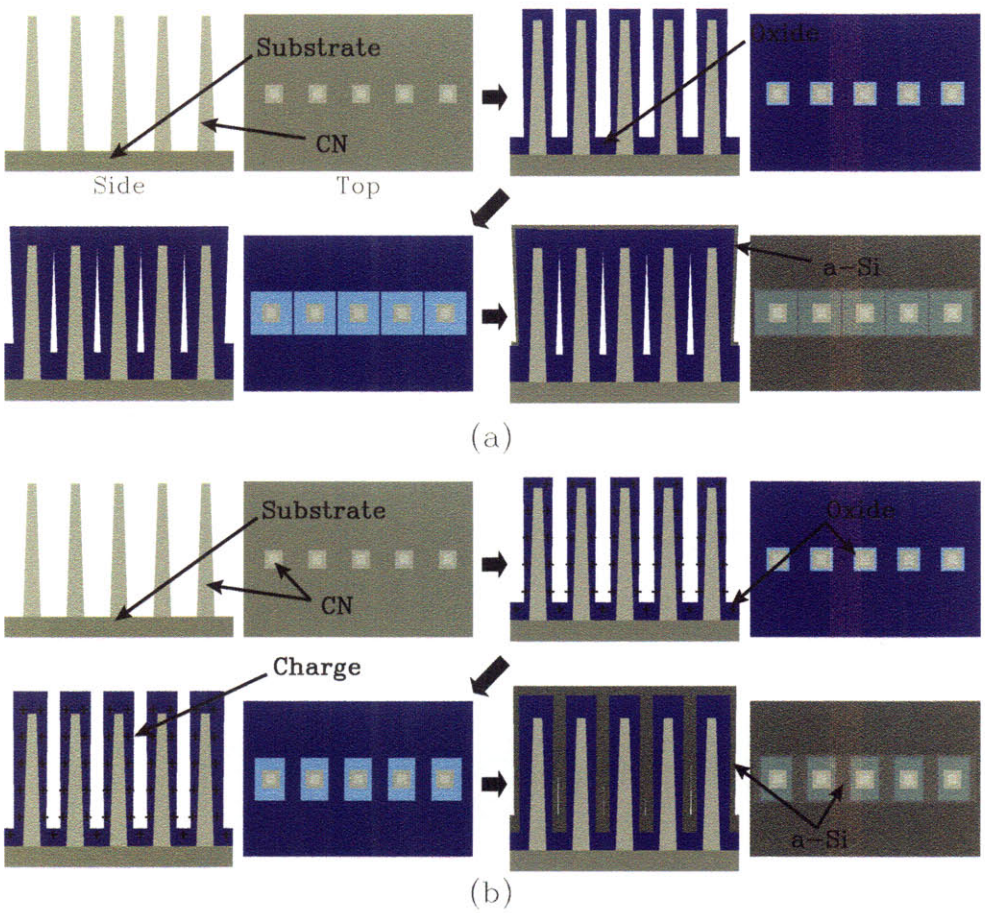


Figure 4-19: Schematic of the two oxide growth models resulting in asymmetric growth and voids, a) the conventional "mushroom" type growth and b) the proposed charge induced asymmetric growth.

ions are double effected by both two charged CNs slowing down the grown rate of oxide and resulting in the oval shaped growth of the oxide. This is shown schematically in Figure 4-19 with a comparison of the two models.

As stated before, in the end a long enough growth will results in a bridged gap.

4.2.3 a-Si Deposition

The P-doped amorphous Silicon (a-Si) contacts are deposited directly after the oxide via PECVD. The source gas for the deposition for the a-Si is SiH_4 and is doped in-situ using PH_3. The sheet resistance of the deposited film is 130.5 $\pm$0.2 $\Omega/$. The resistance of the contacts themselves are controlled via the amount of PH_3 used

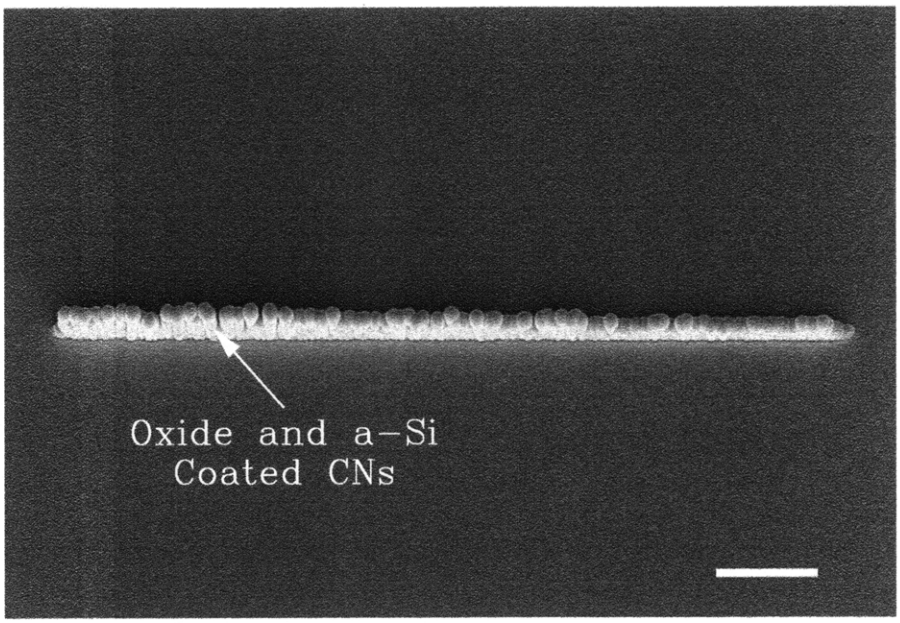


Figure 4-20: Tilted scanning electron micrograph of a row of nanotubes after the oxide and a-Si deposition. The scale bar corresponds to 10 μm.

during deposition. Figure 4-20 shows a scanning electron micrograph of a device at this point in the fabrication.

4.2.4 Self-aligned Spin Planarization

One of the most novel aspects of this fabrication scheme is a spin planarization technique for making self aligned contacts. The typical route to creating contacts would involve a separate masking step aligning a pair of contacts to the nanotubes, assuming the contacts are large, i.e. photolithographically defined, the alignment can at most be within 500 nm of the desired location, which is unacceptable. As stated before the technique used is an adaptation of a previous self-align technique used for making field emitters. [8] Rather than spin a resist to a certain height as was the case of field emitters, a resist is spun that is thicker than the height of the tube. This technique is used instead of spinning to a height less than that of the tubes in order to prevent variation in heights of resist on either side of the line of tubes. This was not a problem with individual tubes since their diameter were small enough that the resist could flow around the individual tubes, but in the case of lines a wall is formed preventing this

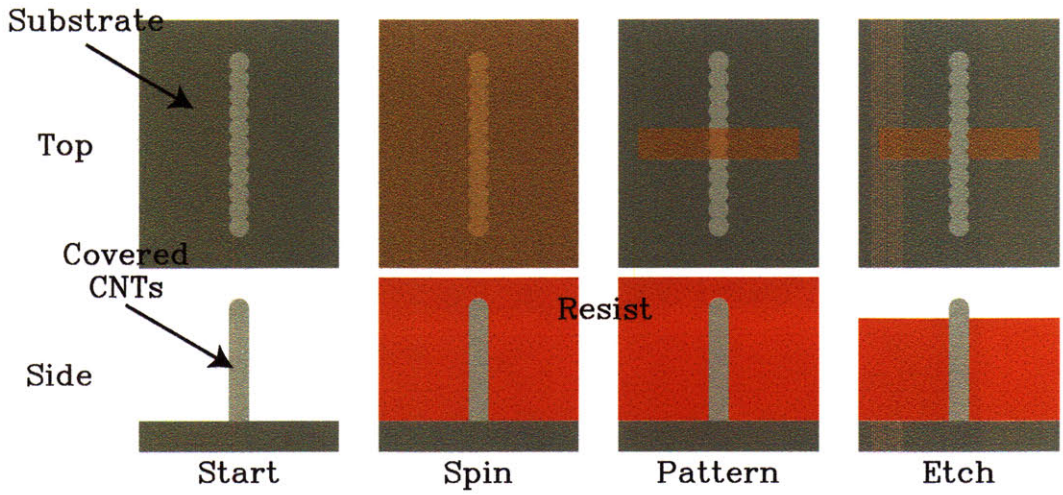


Figure 4-21: Schematic of the self-aligned contacts by spin planarization used in this work.

from occurring and results in visible streaks in the resist. By spinning a layer that is thicker than the height of the tubes, the wafer can be planarized as if the features below it are not even there. At this point a line is patterned perpendicular to the line of tubes for reason previously stated. Finally, the resist is etched to expose the line of tubes. This process is shown in Figure 4-21 and the resulting scanning electron micrograph is shown in Figure 4-22.

4.2.5 Contact Etch

Great pains are taken in the fabrication of most cases of NEMs and MEMs to anisotropically etch materials, this is not one of those cases. Given that the electrodes are created by etching all the a-Si not covered by the resist and that the a-Si is vertically oriented in some places it is important to isotropically etch the silicon. This is accomplished by a high density plasma etch which ensures that the etchant gas, in this gas fluorine, F, will have no preferred direction by the time it reaches the surface of the sample and thereby etching it isotropically.

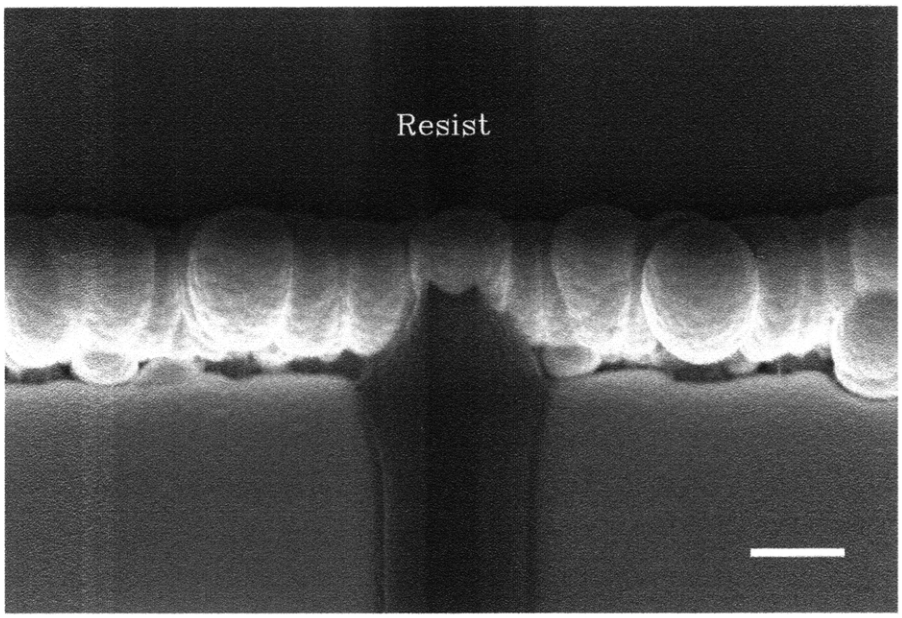


Figure 4-22: Tilted scanning electron micrograph of a device after the reduction in the height of the resist by etching. The scale bar corresponds to 2 μm

4.2.6 Release

The final step in the process is the release of the device through removal of the oxide. Prior to this step a number of other processing can be performed with the device such as the deposition of gold contacts and wire bonding for circuit applications discussed in the next chapter. This is because the oxide encasing prevents any damage to the nanotubes by almost any processing. That being said, the difficulty is then in the removal of the oxide without damaging the nanotubes because of capillary effects.

Initially, vapor HF seemed like the logical choice but unfortunately it was later discovered that vapor HF left residues in nitrogen containing PECVD silicon oxide films as happened to be the case, Figure 4-23 shows the residues left in this process. [16] Successful release of the device was facilitated through the use of buffered oxide etchant and critical point drying which circumvented capillary and surface tension forces from destroying the device.

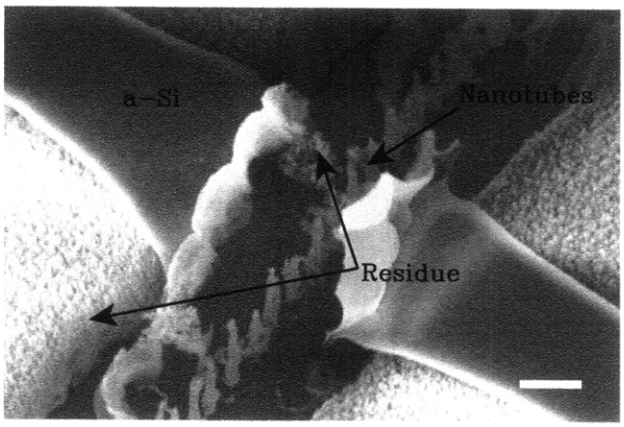


Figure 4-23: Tilted scanning electron micrograph of a device released using vapor HF. The scale bar corresponds to 1 μm

4.2.7 Results

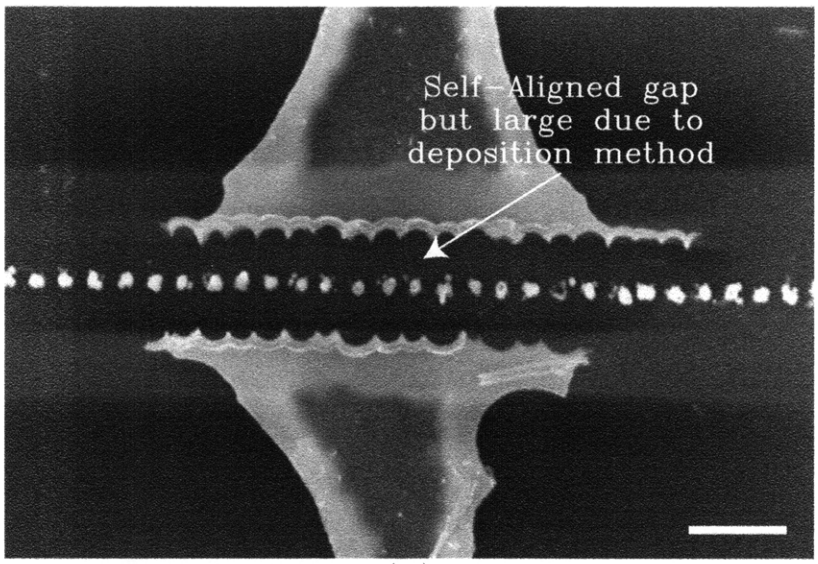
The final fabrication results are shown in Figure 4-24. The Figure highlights some of the issues that still need to be overcome such as large gap sizes and short tubes. Eventually devices with tubes with about 10 μm were fabricated and results for those devices are discussed in the next section.

4.3 Measurements

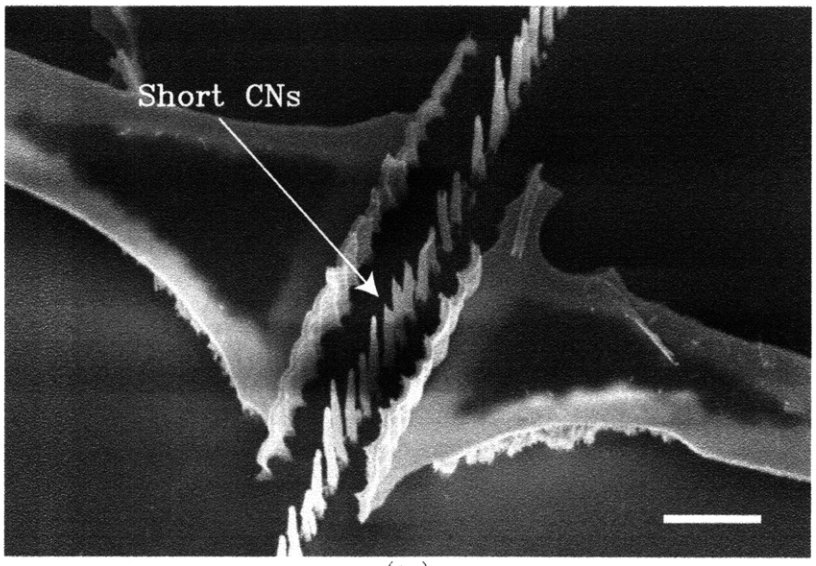
Two sets of measurements were performed. Using a set of tubes with equivalent size, a similar setup as in the previous chapter was used to probe the influence of gap size on the voltage operation of these devices. And the second was a best case scenario device using current fabrication methods.

4.3.1 Voltage vs Gap

These experiments were performed using lines of nanotubes on a substrate right after the growth experiment and were tested in a similar fashion as the two terminal measurements in Section 3.1.3.1 with a few exceptions. First,rather than use an CN attached probes, the CN were electrically contacted via the substrate and a single tungsten probe was brought into contact with the tips of the nanotubes. Second,



(a)



(b)

Figure 4-24: Scanning electron micrograph of a fully fabricated device from the a) top and b) tilt view. The scale bars correspond to 2 μm.

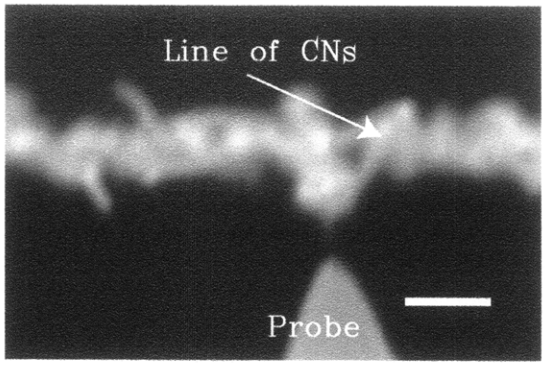


Figure 4-25: Setup for pull-in voltage versus gap measurements using 10 μm nanotubes. The scale bar corresponds to 1 μm

the tungsten probe itself was bent to both fit underneath the objective of the SEM and in doing so the tip of the probe was more or less parallel to the CNs. In this way a better electrostatic control of the CN was able to be obtained and thus more representative of the final device. A top view scanning electron micrograph of a the setup is shown in Figure 4-25. The nanotubes used in this experiment had a height of $L = 10\mu m$ and a diameter of $d = 150 - 180nm$. Two terminal measurements were conducted to determine the pull-in voltage at a varying gap distances. Measurements were done for individual CNs so as to avoid any potential variations in mechanical properties of different CNs. The CNs were pulled into the electrode to measure the pull-in voltage and physically pulled away to release the CN from the probe. The range of motion of the nanomanipulator was restricted to a single axis to ensure that the probe mainted the same capacitance, in terms of area, each time. The results for a CN that lasted for the greatest number of measurements before final failure plotted in Figure 4-26. Since the exact probe area, and Young's modulus for these CNs were unknown, agreement between these results with the previously described theoretical models, see Chapter 2, for a vertical carbon nano-relay structure was judged on the basis of scaling of the measurements and the scaling of the model. [21] In terms of scaling of the model with gap size and the measurements, they show very good agreement.

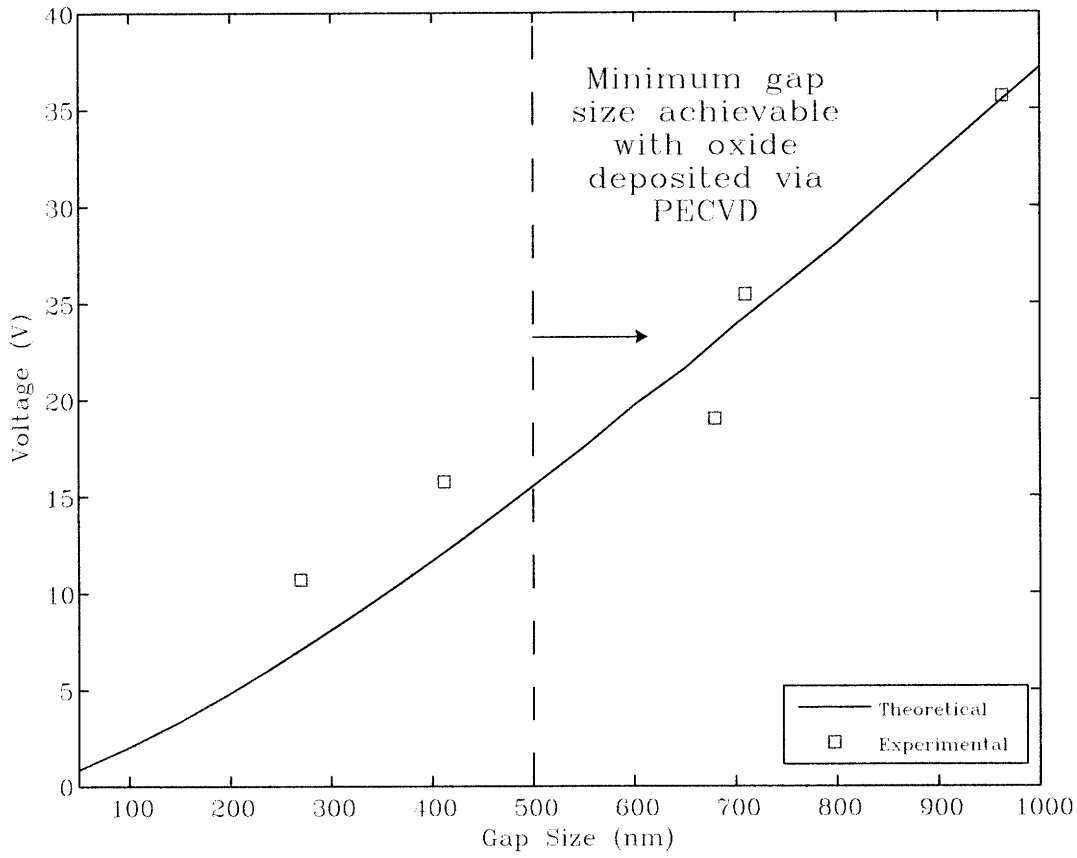


Figure 4-26: Pull-in voltage versus gap size for a single tube. Experimental measurements plotted alongside model.

4.3.2 Best Case

The second measurement performed was a pull-in measurement for a fully integrated device fabricated under the "best case" scenario given the limitations in fabrication previously discussed. As before, pull-in is defined as a sharp transition in current as a result of the nanotube coming into contact with the doped a-Si electrode. The nanotubes in this device had a height of $L = 10\mu m$ and diameter of $d = 150 - 180nm$, and gap distance of $g = 500nm$ between the nanotube and the side electrode. The I-V measurement for the device is shown in Figure 4-27. The measurement was run twice to determine whether or not the nanotube would stick. During the first measurement the sharp transition in the current at - 12 V indicates that the nanotube pulled into the electrode. This result is of the order of what was expected from the previous two terminal measurement, the lower pull-in as compared to the probe measurement (Figure 4-25) in may be a result of either a difference in Young's modulus or a result of increased area of contact between the CN and the contact. During the second run there is no evidence of pull-in and the overlap between the first and second runs is evidence that the nanotubes remains in contact with the electrode due to stiction. Pull-off is not possible at these pull-in voltage. Simply considering the increase in gap size when the CN is pulled-in, one would expect that pull-off would be possible at 40V. Unfortunately close range stiction forces can match or even exceed long distance elastic and electrostatic forces. [31] Therefore, short range stiction forces will account in large part for the the lack of ability to pull-off the CN. Since the magnitude of these forces are relatively unknown, an estimation of the actual pull-off voltage for this system is not possible. Fortunately interaction between these devices are currently a topic of great interest [62], and a method for measuring the stiction forces will be suggested in the future work in order to predict the resulting pull-off voltage.

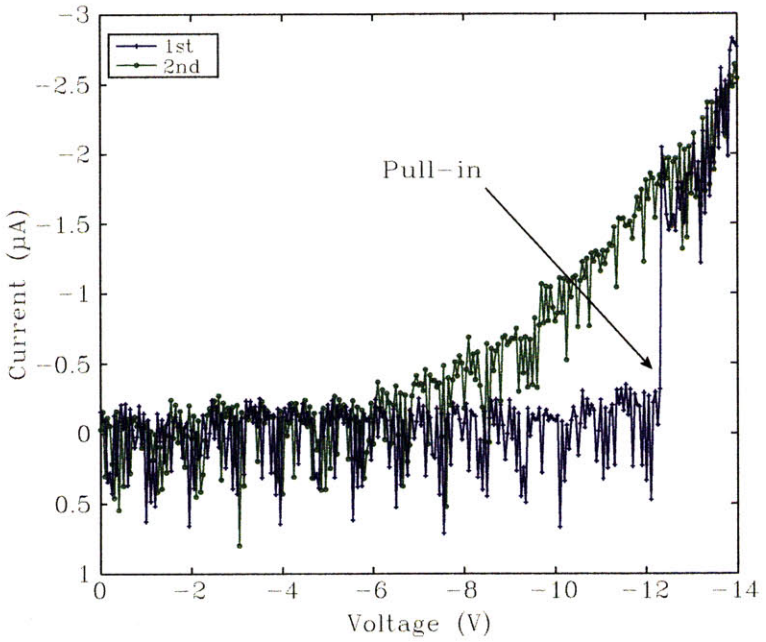


Figure 4-27: I-V plot of a fully integrated device showing pull-in as well as stiction during the second run.

Chapter 5

Double Graphene Switch

5.1 Introduction

Again,although the potential benefit to the subthreshold slope is clear, reliable NEM switches have not been demonstrated with low voltage operation and low contact resistances. [59, 42, 27, 29] One of the leading problems is failure due to irreversible switching, or stiction,[4] which arises primarily from small scale forces, such as van der Waals forces, and capillary forces. The solution that will prevent stiction in this class of devices has been to either to: (i) create structures with large elastic forces to overcome the stiction forces,[49] (ii) avoid direct contact and operate in the regime of tunneling, or (iii) coat contacts with an insulating material to prevent stiction and operate in the regime of tunneling. Unfortunately these approaches result in either high operating voltages or low on current. In the earlier discussion of a vertically oriented carbon nano-relay the primary goal was to use stiction as part of the operating principle of the device, in this chapter a novel double graphene device is discussed with the potential benefits of little to no stiction.

Graphene may help overcome stiction and reliability problems in NEMs. Not only does graphene exhibit exceptional electrical and mechanical properties[7], but graphene's hydrophobicity and the uniquely weak interactions between stacked graphene sheets make it a strong candidate to overcome this issue. These weak interactions between graphene layers are similar to those between carbon nanotubes and graphene-

shells in multiwall carbon nanotubes and have already been exploited to create devices such as nanotube memory elements and bearings for nanorotors. [59, 10, 17, 5, 14] Typically, the deposition of graphene on a surface is performed by mechanically exfoliation of graphene sheets from highly oriented pyrolytic graphite (HOPG) source.[51] Although this technique has yielded graphene sheets with relatively large dimensions, it may not be applicable to the fabrication of large area devices and it is only compatible with a"bottom-up" fabrication approach. [29] Recently it has been shown that graphene films of near arbitrary size can be grown by ambient pressure chemical vapor deposition (CVD). [34, 56] These CVD graphene films consist of multiple domains of single and multilayers of graphene and exhibit many of the qualities of mechanically exfoliated graphene. [34] In addition these films can be transferred to almost any substrate facilitating the use of "top-down" fabrication. In this letter, we present a large area all CVD graphene switches capable of multiple switching.

A schematic diagram of the double CVD graphene switch is shown in Figure 5-1 and the operation of the switch is similar to that of a typical electrostatically actuated NEM swith and is shown in Figure 5-2. A flexible top beam of CVD-grown graphene is suspended above an inflexible bottom film of graphene. There are three contacts: two top contacts made to either end of the top graphene beam, and a bottom contact is made to the bottom film of graphene. The top contacts allow electrical characterization of the flexible top graphene beam. A capacitive force resulting from an applied bias between the top and bottom contacts brings the top beam into electrical contact with the bottom graphene film. When the bias is removed, elastic forces and weak stiction forces allow the top beam to return to its initial position.

5.2 Fabrication

The fabrication process is shown in 5-3. The graphene films used for this device were grown by ambient pressure chemical vapor deposition on thin films of transition metals. [34, 56] The films were grown using a slow cooling method ensuring that up to

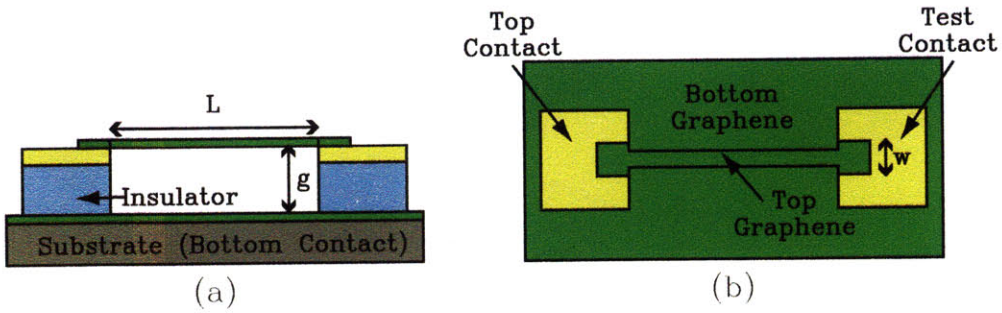


Figure 5-1: Schematic diagram of a double CVD graphene switch shown from a) a cross-sectional view and b) a top down view

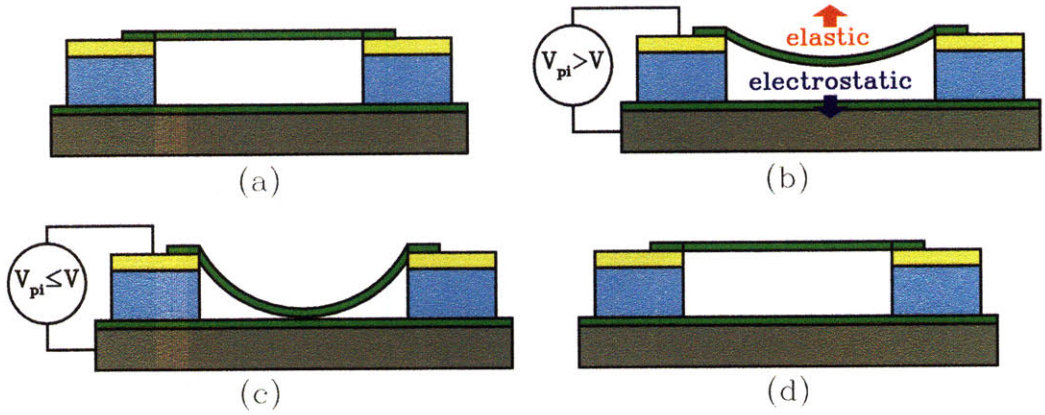


Figure 5-2: Operation of a double layer graphene switch starting from the a) "off", b) then the beginning of the pull-in stage when the applied bias V is less than the pull-in voltage and also showing the forces acting on the top beam, c) the final "on" state when V is greater than or equal to the pull-in voltage, and finally d) the restored "off" state upon removal of the bias.

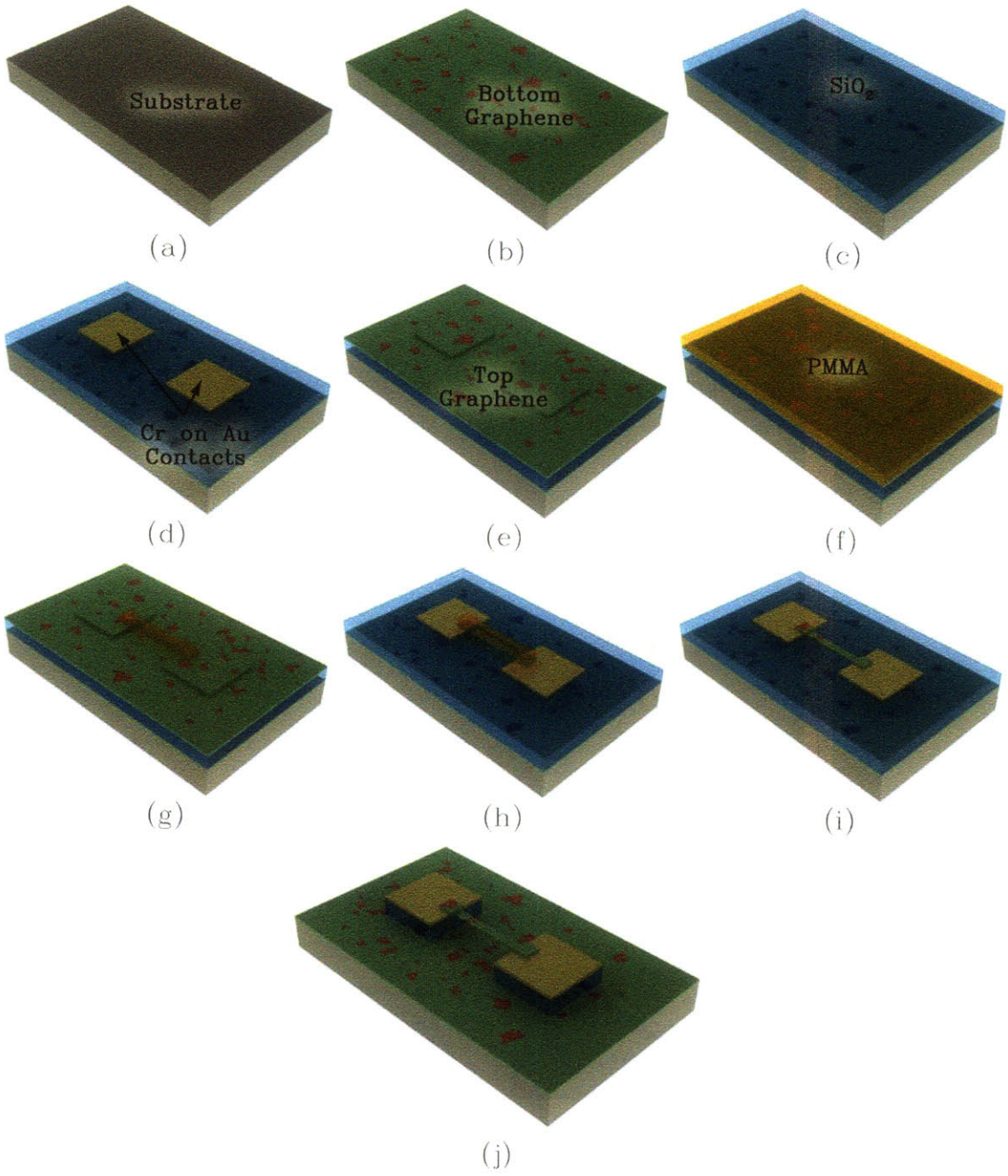


Figure 5-3: Schematics of the fabrication process for a double CVD graphene switch. The following steps are shown: a) doped silicon substrate, b) bottom layer of graphene on the silicon substrate, c) PECVD deposited SiO_2, d) patterned contacts, e) a transfered top layer of graphene, f) the PMMA resist mask, g) patterned PMMA beam, h) pattern transfer of the PMMA beam to the graphene, i) removal of the PMMA, and j) etch and release of the device.

87% of the area is composed of no more than two graphene layers. [57] The technique for transferring CVD graphene layers was similar to that reported for the transfer of large area graphene films onto arbitrary substrates. [56] The process begins with the transfer of a large graphene film on to highly-doped silicon substrate (Figure 5-3a), which performs the function of a large area contact to the graphene (Figure 5-3b). A 500nm thick silicon dioxide layer, SiO_2 is deposited using plasma enhanced chemical vapor deposition (PECVD) (Figure 5-3c). The top and test contacts, 7 nm Cr / 50 nm Au, were then patterned on the surface of the SiO_2, Figure 5-3d. A second graphene film is transferred on top of the insulator/contact stack (Figure 5-3e). A 500nm thick layer of 495k PMMA is spun on the sample (Figure Figure 5-3f), and beams of lengths and widths ranging from 5-50 μm and 3-10 μm, respectively, are photolithographically patterned using a deep ultraviolet (DUV) light source (Figure 5-3g). The beams patterns are transferred to the top graphene film using oxygen plasma (Figure 5-3h). [45] Finally the PMMA mask is dissolved away using acetone (Figure 5-3i) and the regions of the SiO_2 not masked by the top and test electrodes are etched by a combination of dilute hydrofluoric acid (HF) and critical point drying (CPD) (Figure 5-3j). [15, 20] Photomicrographs and electron micrographs of a few key steps are shown in Figure 5-4. The integrity of the fabricated devices are then electrically examined by measuring the I-V characteristics between the top and test contacts. Figure 5-5 shows the similarities in the I-V characteristics of devices before and after the removal of the oxide layer indicating that very little, if any, damage is incurred by the graphene sheet. This method is employed since the suspended devices are optically transparent and scanning electron microscopy was avoided to reduce the risk of damage or contamination to the graphene layers. We observed that many of the larger devices do not survive the final step and are torn apart but the thinner, $w < 3\mu m$, beams remain intact. Similar results have been reported for suspended HOPG-based graphene devices. [15, 20]

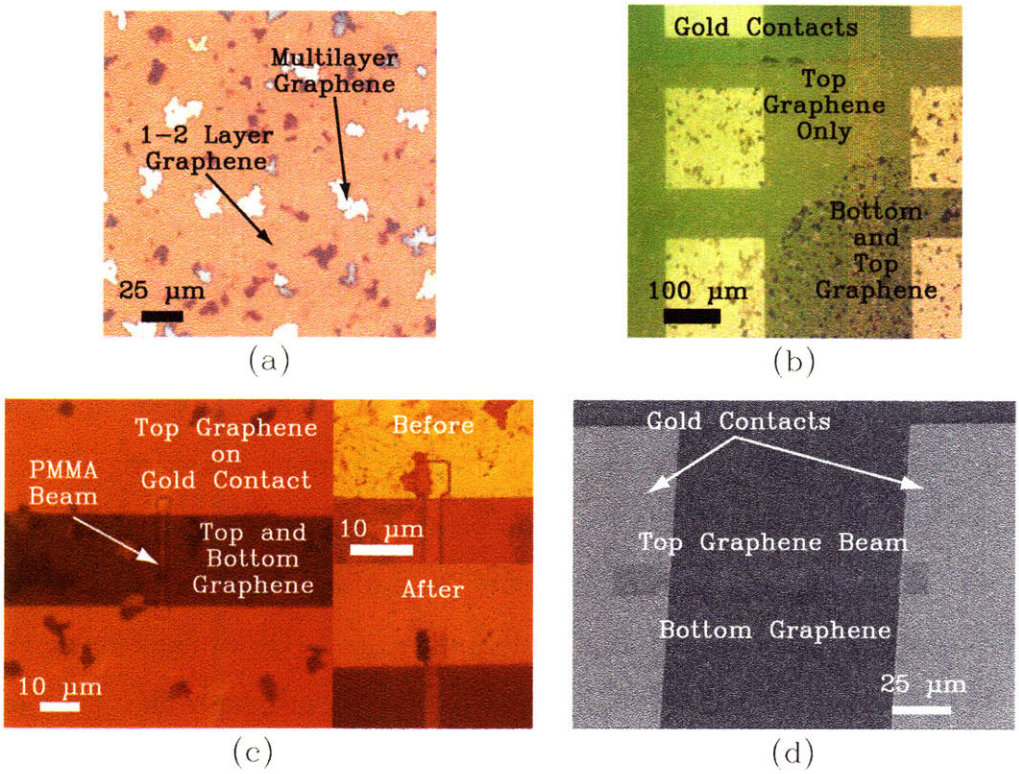


Figure 5-4: Photomicrographs of a) a typical CVD grown graphene film showing domains of 1-2 and multilayer graphene growth, b) a double CVD graphene device after the second or top layer of graphene has been transfered with various areas containing no graphene, just the top graphene and both the top and bottom graphene layers, c) (left) a patterned PMMA beam on the top graphene and (right) the transfer of that beam to the bottom graphene after an oxygen plasma etch and finally d) an electron micrograph of a completed device.

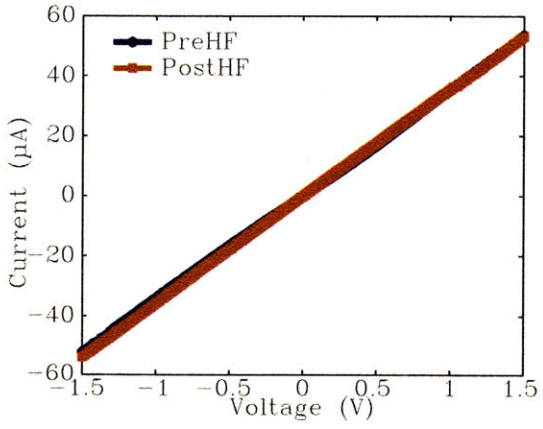


Figure 5-5: I-V measurements between the top and test electrodes of similar devices before and after the final step in the fabrication process, the HF etching of the oxide.

5.3 Results and Discussion

The electromechanical properties of the double graphene switches were examined by measuring the current between the top and bottom electrodes, while sweeping voltage between the two electrodes from 0 to 5V. The typical I-V behavior of these devices is shown in Figure 5-6. For the initial switch measurements, the switching results in a sharp increase, at 4.5 V, in the current as a result of the top graphene beam coming into contact with the bottom graphene film. The hysteretic behavior as the voltage is swept from 5 to 0V indicates that the top graphene beam remains in contact with the bottom graphene film until the applied bias is removed. Once the applied bias is removed the top graphene layers comes out of contact with the bottom graphene due to an elastic restoring force. This measurement is repeated several times until the top graphene beam comes into permanently contact with the bottom graphene film. Once this occurs a subsequent I-V measurement shows no hysteretic behavior as seen in line iii of Figure 5-6. For the device used to obtain the results in 5-6 the device was able to switch several times before the top layer of graphene came into permanent contact with the bottom layer.

Ultimately, these devices fail due to mechanical fracture of the graphene film causing the top graphene to tear and contact the bottom graphene layer creating a short. It is appears that the graphene films tears along the boundaries of the graphene domains. The tear in the top graphene that created the short for the device in Figure 5-6 is shown in Figure 5-7b. The onset of this failure is evidenced in the I-V of a run right before failure, seen in line iii of Figure 5-6, by the sporadic behavior seen as the top graphene beam is pulled down. This mechanical failure is also reflected in the conduction of the top graphene layer itself. The I-V data shown in Figure 5-7a shows the change in resistance of the top graphene beam, obtained by applying a bias across the top and test electrodes, before the first run and after the final run. The increase in resistance is a result of a decrease in effective beam width caused by the tear. Presently the subject of further study with these devices is the increase in mechanical robustness both through device scaling as well as the use of newer CVD

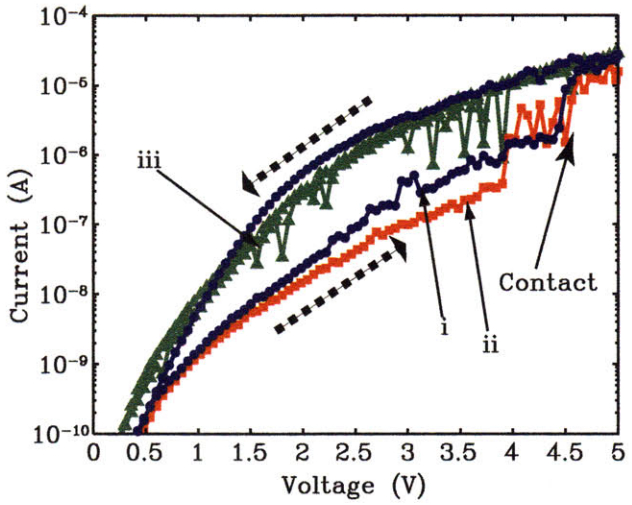
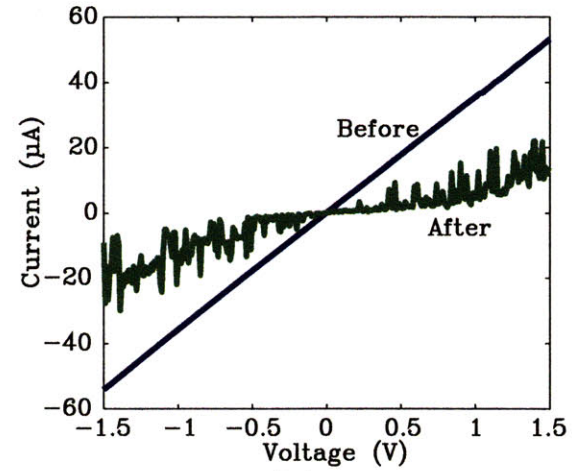


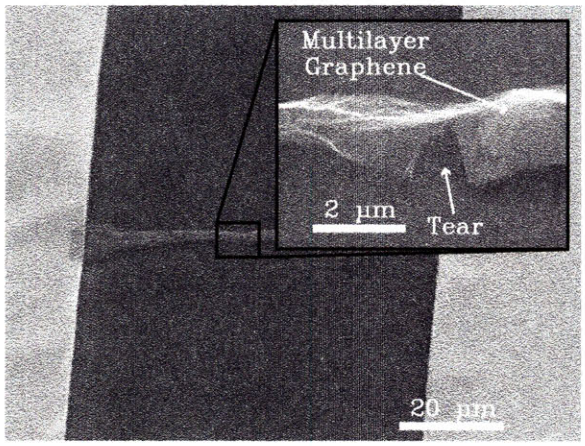
Figure 5-6: Current-Voltage characteristics between the top and bottom contacts for a w=3μm, L=60μm, and g=500nm device showing multiple events of switching. i) First scan, ii) Third scan (from 0 to 5V only), and iii)the fourth and final scan.

graphene films with larger graphene domains.

Similar to results previously reported the graphene films exhibit excellent electronic properties. The sheet resistance as measured between the top contacts was found to be between 900-1100 Ω/sq. Assuming a worst case scenario, with an average cross-sectional thickness of 3 nm [56] in the non 1-2 layer region (Figure 9-1), these films were able to accommodate current densities in excess of 7 kA/cm^2 making them extremely robust electrical conductors. The on current is 10 μA/μm at 5 V and is limited by a contact resistance of $<$ 200 kΩ between the top and bottom graphene layers. We expect that the contact resistance is presently limited by the non-uniform surface of the CVD-grown graphene. The off current is primarily due to leakage through the PECVD oxide.



(a)



(b)

Figure 5-7: Electrical and physical evidence of mechanical failure in large area CVD graphene switches. a) I-V data of the graphene beam measured through the Top and Test contacts before switching measurements and after switching measurements. b)Scanning electron micrograph of device after testing. Inset is a magnified image of tear in graphene beam.

Chapter 6

Conclusion

Power dissipation primarily due to leakage in the subthreshold region is the biggest problem facing the semiconductor industry. Through an analysis of voltage-gated ion channels, NEMs switches are the answer to this problem. The most important problem facing the realization of NEMs today is failure due to stiction. We have successfully demonstrated two large-area devices to solve this key issue in NEMs, the first being a design approach that operates by stiction and the second using a materials approach to minimize stiction. Each device is unique and offers its own advantages and disadvantages.

Our first approach, a vertically oriented carbon nano-relay, employed a vertically oriented CN between two contacts. The device operates on the principle that the CN will stick to the electrode on contact, but this stiction is reversible through the application of a bias with an opposing electrode. Using a nanomanipulator in tandem with a CN attached probe a device operating with reversible stiction was shown. The concept was then employed to create a wafer integrated large-area device. Pull-in operation was demonstrated with the integrated device below 13V. Upon re-testing the device the absence of switching behavior showed the stiction of the CN to the device, proving the concept of a vertically oriented carbon nano-relay can be integrated on a wafer. Optimization in fabrication is still required to combine the concepts of pull-off operation in an integrated device.

Our second approach, a double graphene switch, employed two stacked layers of

CVD grown graphene films as low-stiction materials for electromechanical switching. These large-area devices exhibited the ability to switch multiple times at applied biases below 5V with failure caused by stiction. Rather, the failure mechanism of these devices arises from fracture of the polycrystalline graphene films. The absence of crystalline domain boundaries within the active area of the device may increase the reliability.

Although the field of NEMs is still relatively new and filled with a variety of challenges, such as reliability, both these design approaches have successfully demonstrated the ability to circumvent the leading problem of NEMs stiction. Having solved this critical issue we can start to now look at NEMs at least as a potential tool to addressing the subthreshold leakage based power dissipation problem plaguing the semiconductor industry today.

Chapter 7

Future Work

7.1 Vertical Carbon Nano-Relay

7.1.1 Fabrication

The obvious next step for the vertical carbon nano-relay is the lowering of the pull-in voltage in order to facilitate pull-off in the integrated device. Because of the self-aligned nature of the fabrication, it is still the best route towards the creation of an integrated device with a few minor tweaks, of course.

7.1.1.1 Carbon Nanotube/Fibre

Going back to Equation 2.19, the one route to lowering the pull-in voltage that was not investigated was trying to decrease the tube diameter. Although, from Figure 4-9, this does not seem to be a lithographically tailorable parameter, from Table 4.1 this could be accomplished through the use of a different catalyst such as iron, Fe. The smaller diameter results in a shorter tube height, but the ratio of tube length/height to diameter will likely be higher for Fe than Ni because of its lower sputter rates. For example, at an $E = 500$eV for argon ions at 1 mA/cm^2 the sputter rates for Fe and Ni are 429 Å/min and 570 Å/min, respectively.[19]

Another possibility is to use the same system but to increase the growth rate of the CNs by further increasing the growth temperature[43, 35], again, changing the

catalyst, optimizing other growth parameters such as gas ratios[53] and plasma conditions, or even newer PECVD growth techniques utilizing higher density plasmas[69].

7.1.1.2 Gap Size

The gap size can be reduced to the minimum gap size, g_{min}, discussed in Section 4.2.2 through the use of more conformal oxide techniques. The options cannot include any process that expose the sample to a high temperature oxygen environment which would destroy the CNs, a couple possibilities are TEOS, high density plasma deposition such as an inductively coupled plasmas (ICP) or electron cyclotron resonance (ECR) reactive plasma system, and atomic layer deposition (ALD). Alternatively, the use of high temperature oxygen environments are possible if a thin protective layer of silicon dioxide were initially deposited by PECVD, and then subsequently increase in thickness by almost any other conformal oxide deposition technique.

7.1.2 Architecture for CMOS

To realize complementary logic operation, it is necessary to also insert an additional contact. The new design is shown schematically in Figure 7-1. The vertical orientation of the CNTs should enable the fastest possible switching for a given footprint. Fabrication for a device is similar to that used for the three terminal relay described in Chapter 4 with the exception of an additional oxide and doped a-Si growth after the etching of the initial a-Si layer.

7.2 Double Graphene Switch

7.2.1 Reliability

One of the primary pitfalls of the double graphene switch was the mechanical failure of the graphene beam. Since graphene itself has quite robust mechanical properties[7], the likely cause of failure was the tearing along the grain boundaries of the polycrystalline graphene films. A solution to this problem would be to create a device whose

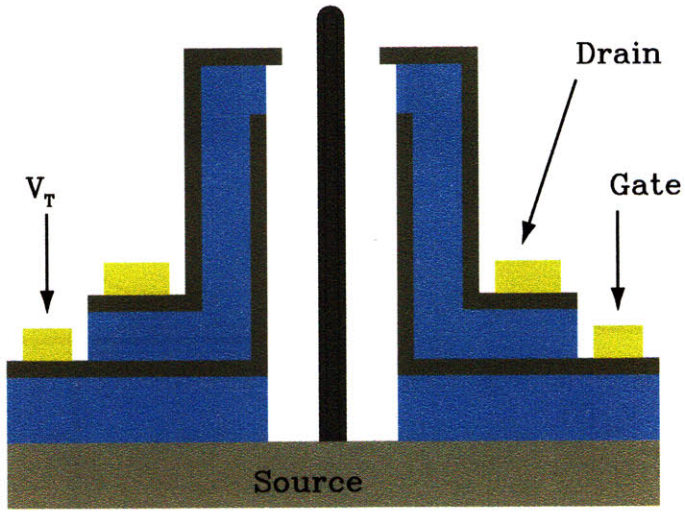


Figure 7-1: For complementary logic a fourth terminal is required to pull the tube off the drain when $|V_{GS}| < |V_T|$

dimensions are less than that of a single graphene. Since the graphene domains are on the order of 5 to 10 μm in length and width a device with ¡ 1 μm in length would work. Statistically, if enough device were fabricated, a few of those devices would consist of a single graphene domain. The alternative solution is to wait until the growth of graphene by ambient pressure CVD matures to the point where large area, single sheets of graphene are made. The prior seems like the prefered solution.

7.2.2 Noise

The other issue with the double graphene switch were the large fluctuations, or noise, in the I-V data in Figure 5-6. I-V data from similar devices, such as the data for a three terminal carbon nanotube base relay[42] shown in Figure 7-2, in fact relatively speaking the data is considerably less noisy. Nonetheless, the origins of noise are likely similar to those for the carbon nanotube based relay, since both techniques employ the use of a transfer rather than direct growth technique. The fluctuations are attributed to contamination on the surface of the CNTs. [42] Although, the transfered graphene layers are thoroughly cleaned in solvent, followed by an cleaning step in a tube furnace at 350 °C under a flow of 15 % hydrogen in argon, it is likely that there are residual traces of PMMA on the surface of the graphene. New transfer techniques

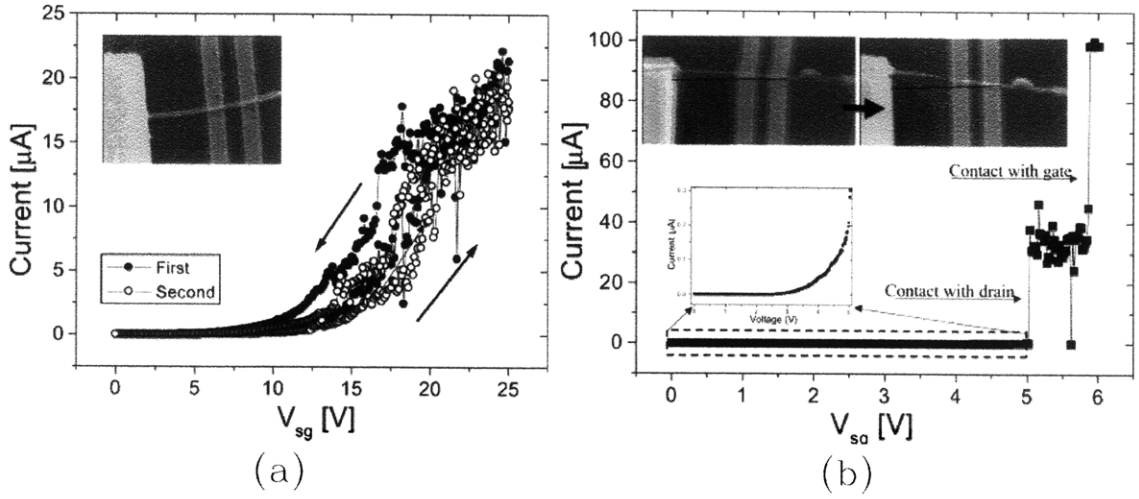


Figure 7-2: Example data extracted from works by Lee et al.[42] Data is presented here to highlight the noise observed in carbon nano-based relays. a) $I - V_{sg}$ data for device with multiple switching events, and b) $I - V_{sg}$ data for device which operated for a single switching event.

with polydimethylsiloxane (PDMS) are being used for transfering graphene for large area, transparent electrodes for photovoltaics have shown to relatively contamination free and is a possible solution.

7.3 Nanomechanics and Surface Forces

The validity of a continuum mechanics model for NEMs was partially shown in Section 4.3.1 by comparing trends in the continuum mechanics model with experimental values for a gap experiment. Given the unknown mechanical and surface properties of the nanostructures used and the range of values possible with nanoscale materials[60, 46, 41, 39], a greater knowledge of these properties to either complete validate these continuum mechanics models. A previously proposed method for measuring surface forces suggested that these values can be measured electrically [2], but this method assumes that continuum models are already valid for both pull-in and pull-off actuation. To accurately determine the validity of any model proposed, it is important to directly measure the mechanical properties of the device being measured. Atomic force microscopy seems to be an idea candidate it has not only been used to measure the nanomechanics of these structures [40], but can also do so non-

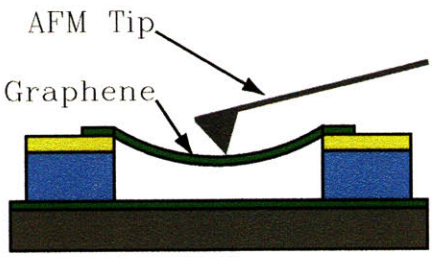


Figure 7-3: Schematic of a graphene film being mechanically tested in a double graphene switch, prior to electromechanical testing.

destructively. Figure 7-3 is a schematic of how this might be accomplished in practice with a double graphene switch. Similar these AFM techniques can also be used to gauge stiction forces in these materials as well.[62]

7.4 Subthreshold and Multiple Charges

The purpose of this work was in large part to provide a toolkit for investigating NEMs as a potential solution for solving the subthreshold problem. Now that a few potential devices have been designed, fabricated and tested, both still need to be optimized to be mechanically reliable. These optimizations aside, the fundamental questions of fixing multiple charge and subsequent effect on subthreshold slope still need to be investigated. Both graphene and CNs are candidates since research has shown that both these materials are easily functionalizable with charges.[54, 66] Initially, influence of these charges should be measurable by investigating the pull-in behavior, for example the pull-in will depend on the sign of the applied bias where as the pull-in of a neutrally charged device only depends on magnitude of the applied bias. The true answer to the subthreshold properties of these devices will continue to remain unanswered until devices are scaled down far enough where thermal fluctuations of the actuator can be significant enough to overcome even the restoring elastic forces and subthreshold effects will be significant.

Chapter 8

Appendix A: Circuit Integration

Note: The circuit design work presented in this chapter applies for devices with pull-off based operation such as the vertically oriented carbon nano-relay and was part of a collaboration with Courtney Schmitt and Anantha Chandrakasan of the Digital Integrated Circuits and Systems Group at MIT. This chapter presents a summary of that work and details regarding the circuit design can be found in Courtney Schmitt's masters thesis. The primary purpose of this chapter is to highlight some unique applications as further motivation for future research of vertically oriented carbon nano-relays with pull-off based operation.

8.1 Circuit Applications

As noted, one of the advantages of NEMs based relays are their low off state currents. Although this is beneficial in a variety of applications, the primary use can be seen in low-power circuits especially in areas where losses due to static power dissipation are relatively high. Also, due to their mechanical, and thus slow, nature these devices are most suited in low to moderate frequency designs. In this chapter several circuit applications for a three terminal vertically oriented carbon nanorelay are examined: reconfigurable interconnects, power-gating and nonvolatile memory.

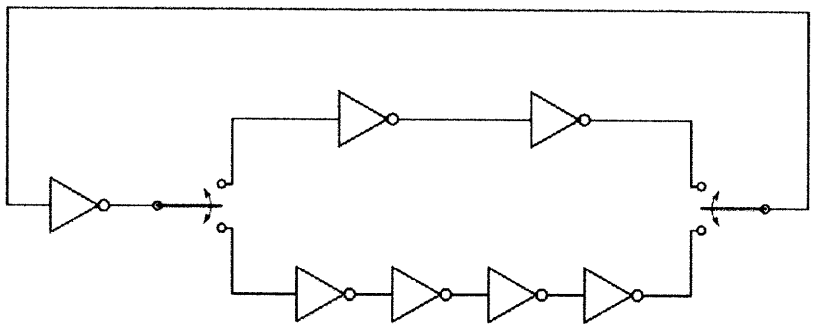


Figure 8-1: Circuit diagram of a ring oscillator implementing a nano-relay as a reconfigurable interconnect.

8.1.1 Reconfigurable Interconnects

Probably the most natural application for vertically oriented carbon nano-relays are as reconfigurable interconnect. A proof-of-concept reconfigurable interconnect circuit is shown in Figure 8-1. In this circuit, the carbon nanotube-based relay is used to choose between long and short delay paths in a ring oscillator in order to program the frequency of oscillation. This application can be expanded to a very low-power field-programmable gate array (FPGA) by using carbon nanotube-based relays within the FPGA switch blocks.

8.1.2 Power-Gating

In the power gating application, the carbon nanotube-based relay is used as a footer switch for a CMOS load circuit, as shown in Figure 8-2. The carbon nanotube-based relay reduces the leakage current of the load circuit when the circuit is not in use. During normal circuit operation, the relay acts as a normal wire connecting the supply voltage to the load circuit. If the circuit is idle, the carbon nanotube-based relay is switched to the off position to disconnect the supply voltage. The virtual supply node at the bottom of the load circuit floats to an intermediate voltage, decreasing the VGS and VDS voltages across the transistors, which reduces the leakage current. Additionally, the air gap of the carbon nanotube-based relay creates an open circuit in the supply path to further decrease the static power dissipation.

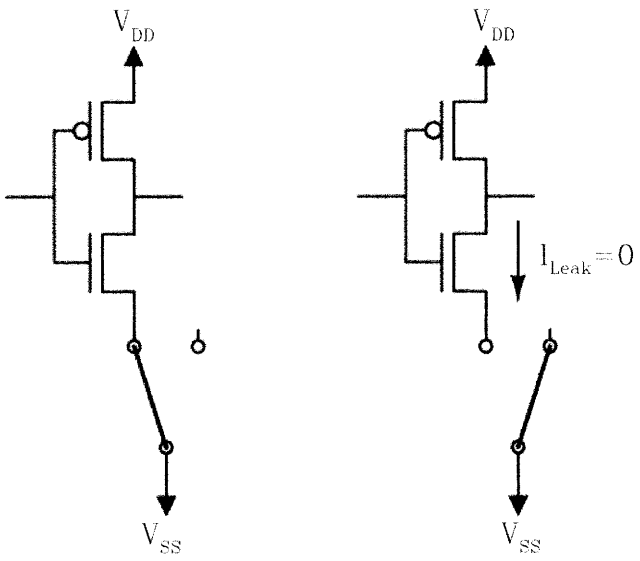


Figure 8-2: Circuit diagram of a power gate.

8.1.3 Nonvolatile Memory

The carbon nanotube-based relay can also be used to construct a nonvolatile memory cell, Figure 8-3. This memory cell was designed by replacing the two cross-coupled inverters of a traditional 6T CMOS SRAM cell with the carbon nanotube-based relay. As in the 6T design, the memory cell is programmed by controlling the word and bitline voltages. However, the state of the cell is held by the position of the relay instead of the voltages on the internal nodes. Since the carbon nanotubes within the relay are held to the contact terminals by van der Waals stiction forces after the control voltage is removed, this is a nonvolatile cell that holds its state without supply power.

8.2 Packaging

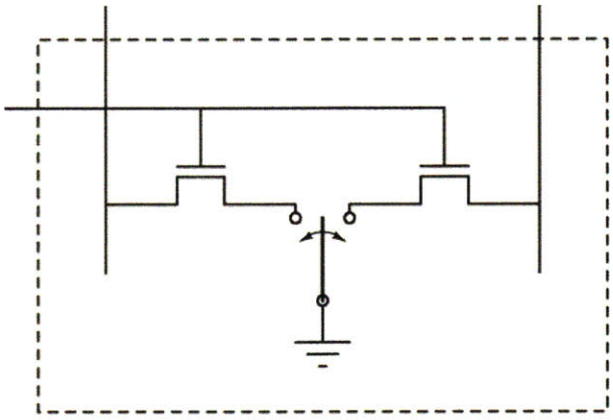


Figure 8-3: Circuit diagram of a nano-relay based nonvoatile memory cell.

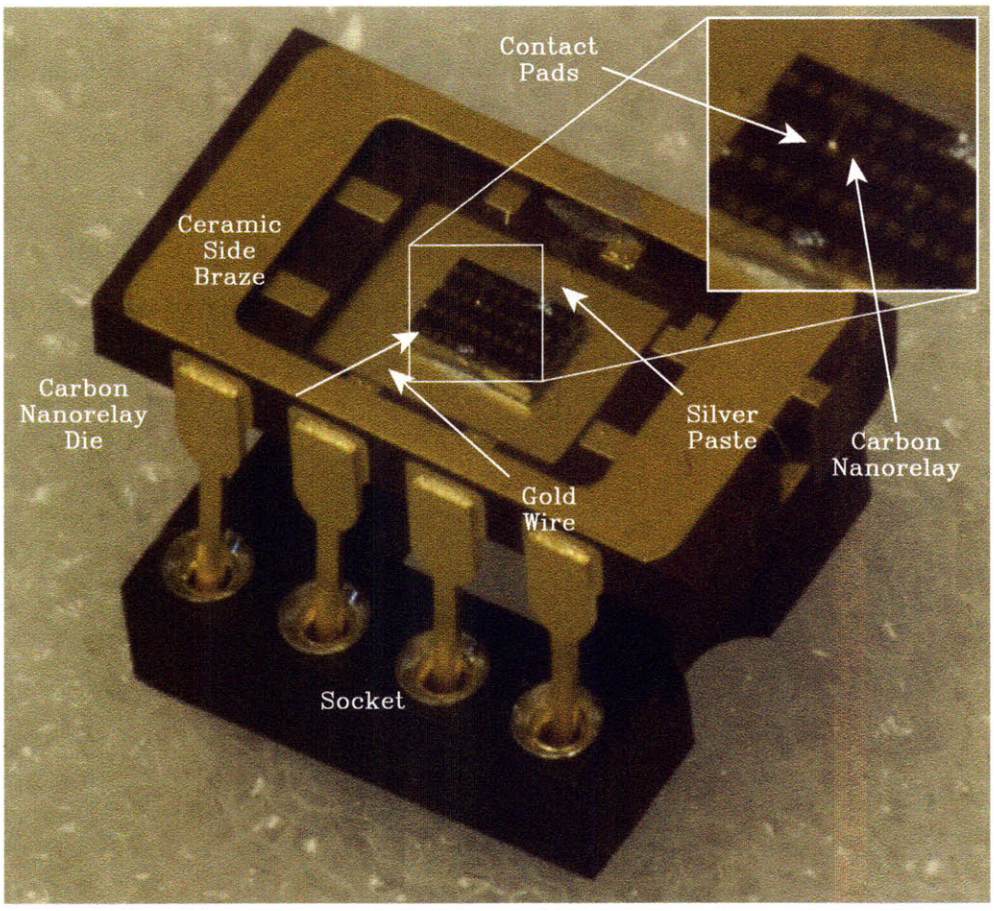


Figure 8-4: A carbon nanorelay delay epoxied in the cavity of a ceramic side braze and wirebonded.

Chapter 9

Appendix B: Figures

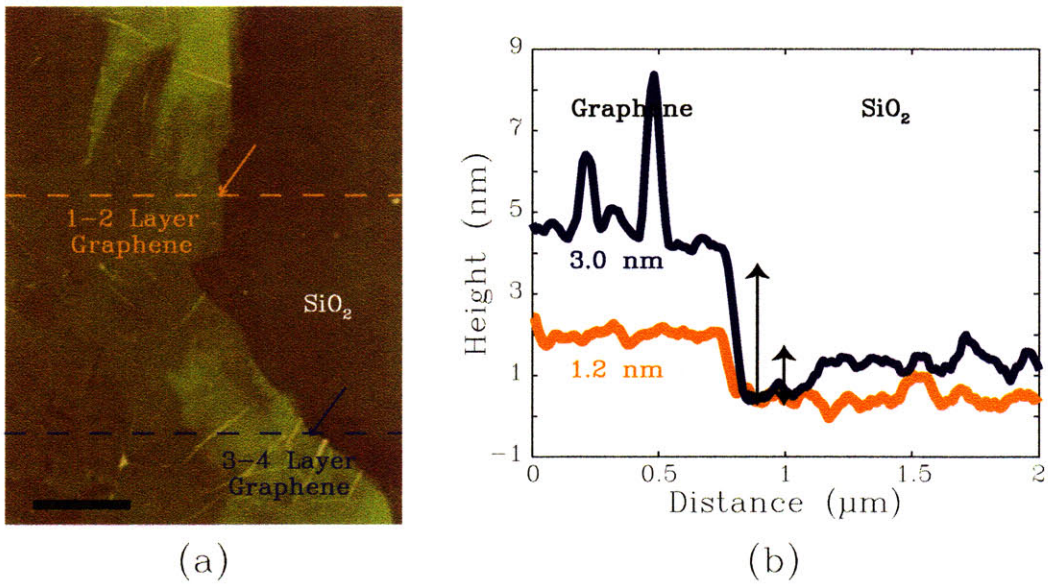
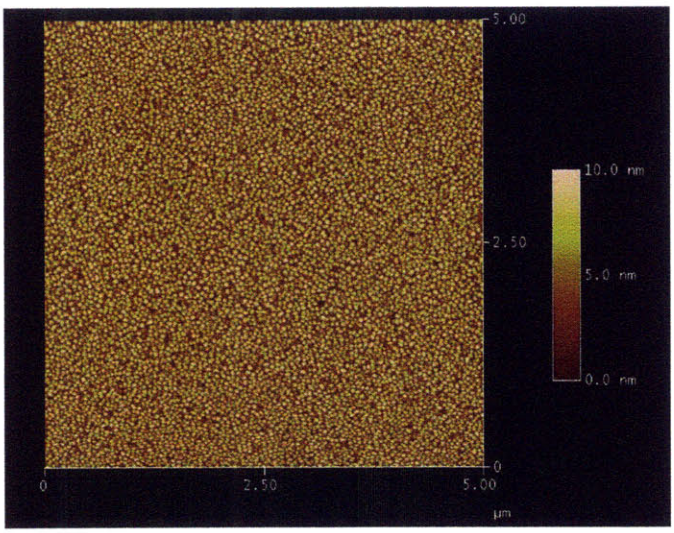
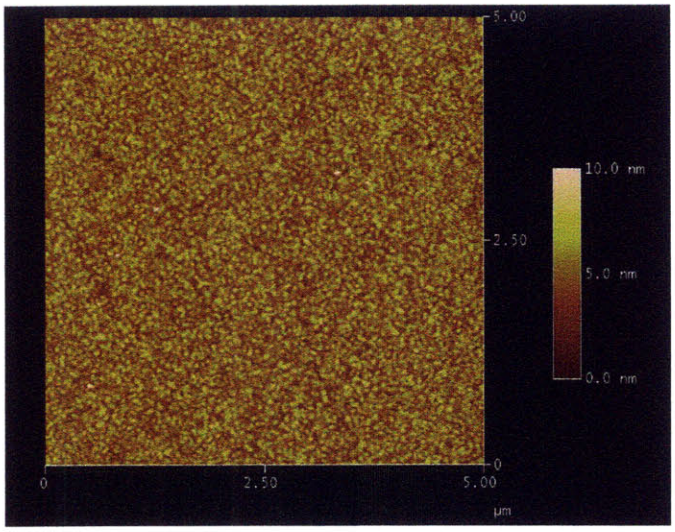


Figure 9-1: Measurement of CVD graphene thickness. a) AFM micrographs of a CVD graphene sheet on SiO_2 showing regions of varying thickness graphene and bare SiO_2, b) step height measurements by AFM of the graphene thickness taken at regions indicated by the lines and arrows. The scale bar corresponds to 1 μm.[56]



(a)



(b)

Figure 9-2: AFM micrographs of Cr/Au gold contacts a) before and b) after annealing.

Chapter 10

Appendix C: Tables

Step	Process	Machine	Figure
1	Piranha Clean	premetal-Piranha	-1
2	Deposit 50nm TiN	endura	
3	Deposit 20nm Ti, 80nm Au	eBeamFP	
4	Photo - HMDS	HMDS	
5	Photo - Spin Resist	coater	
6	Photo - Prebake	prebakeovn	
7	Photo - Exposure	EV-LC	
8	Photo - Develop	photo-wet-r	
9	Photo - Postbake	hotplate	
10	Etch Au	acidhood	
11	Spin Resist	coater	
12	Diesaw	diesaw	
13	Photo - Strip Resist	photo-wet-r	
14	Etch Ti	acidhood	
15	eBeam - Spin Resist	PMMA-spinner	-2
16	eBeam - Prebake	hotplate	
17	eBeam - Exposure	Raith	-3

Continued on next page

Table 10.1 – continued from previous page

Step	Process	Machine	Figure
18	eBeam - Develop	photo-wet-r	
19	Deposit 10 nm Ni	eBeamAu	-4
20	Liftoff Ni	photo-wet-Au	-5
21	Grow CNT	CCNT	-6
22	Deposit Oxide	sts-CVD	-7
23	Deposit doped a-Si	sts-CVD	-7
24	Photo - HMDS	HMDS	
25	Photo - Spin Resist	coater	-8
26	Photo - Prebake	prebakeovn	
27	Photo - Spin Resist	coater	
28	Photo - Prebake	prebakeovn	
29	Photo - Exposure	EV-LC	-9
30	Photo - Develop	photo-wet-r	
31	Photo - Postbake	hotplate	
32	Etch doped a-Si	plasmaquest	-10
33	Photo - Strip Resist	asher	-11
34	Etch Oxide	NSL-innerlab	-12
35	Critical Point Dry	NSL-cpd	
	Optional:		
34	Photo - HMDS	HMDS	
35	Photo - Spin Resist	coater	
36	Photo - Prebake	varTemp	
37	Photo - Exposure	EV-LC	
38	Photo - Post-expose-bake	varTemp	
39	Photo - Flood Exposure	EV-LC	
40	Photo - Develop	photo-wet-r	

Continued on next page

Table 10.1 – continued from previous page

Step	Process	Machine	Figure
41	Deposit 20 nm Ti, 80nm Au	eBeamFP	
42	Liftoff Ti-Au	photo-wet-Au	
43	Etch Oxide	NSL-innerlab	-12
44	Critical Point Dry	NSL-cpd	

Table 10.1: List of Procedure and Tools used in the ICL, TRL, and NSL Fabrication Facilities at MIT

Chapter 11

Appendix D: Fabrication

11.1 Fabrication of an Integrated Vertically Oriented Carbon Nanorelay

The overall fabrication was outlined in Chapter 4. Here the fabrication is given in detail for anyone wishing to reproduce the device. An attempt is made to describe the process so that any individual with access to a fabrication facility will be able to reproduce the results, but unfortunately certain steps are more relevant to those individuals with access to machines noted in Table 10.1 in the Microsystems Technology Lab facilities at the Massachusetts Institute of Technology.

11.1.1 Catalyst Diffusion Barrier

1. Start with a prime 100mm P/B (100) 525μm 0.01-0.02 ohm-cm SSP wafer.
2. Piranha clean wafers in a 1:3 H_2O_2:H_2SO_4 solution for 10min. Dump rinse wafers 4 times.
3. Strip residual oxide in a 50:1 H_2O:HF solution for 15sec. Dump rinse wafers 4 times follow with a spin rinse and dry cycle.
4. Sputter deposit 500ÅTiN. Note: Care is taken minimize time between wafer clean and sputter deposition.

11.1.2 Photoalignment Mask Layer

5. Deposit sub/20nm Ti/100nm Au . Note: Care is taken minimize time between sputter deposition and subseqent sputter or e-beam deposition.

   (a) Sputter deposition. Start with a vacuum pressure <3e-6Torr. Deposit Ti at a power of 1kW for 2 minutes (23nm). Deposit Au at a power of 1kW for 2 minutes (95nm).

   (b) E-beam deposition. Start with a vacuum pressure <1e-6Torr. Deposit Ti at a rate of 1Å/s. Deposit Au at a rate of 3Å/s.

6. Treat wafers with HMDS primer by using a standard vacuum vapor primer oven.

7. Spin on OCG825 resist on wafers by first dispensing resist on wafers spinning at 500rpm for 3sec, then spreading the resist at 750rpm for 3sec and finally thinning the resist by spinning at 3000rpm for 30sec.

8. Bake in an oven at 90°C for 30 minutes.

9. Expose alignment marks using a contact aligner with a chrome photomask in hard contact. Expose with a 365-405nm 10mw/cm^2/sec light source for 2.5sec.

10. Develop in OCG 934 1:1 for 80sec by placing wafer in developer and then agitating the developing solution. Follow developing with a DI water rinse for 1min and N_2 blow dry.

11. Bake in an oven at 120°C for 30 minutes or hotplate at 140°C for 2min.

12. Wet etch gold using Type TFA: 28Å/sec Gold Etchant from Transene Company for 30-35sec by placing wafer in etchant and agitating. Follow with a DI water rinse for 1min and N_2 blow dry.

13. Wet etch gold using Type TFT: Titanium Gold Etchant from Transene Company for 30-35sec by placing wafer in etchant and agitating. Follow with a DI water rinse for 1min and N_2 blow dry.

14. Solvent clean wafers by washing in acetone for 1min, isopropanol for 1min, methanol for 1min, and DI water for 1min while making sure that the solvents do not evaporate between wash steps.

15. Treat wafers with HMDS primer by using a standard vacuum vapor primer oven.

16. Spin on OCG825 resist on wafers by first dispensing resist on wafers spinning at 500rpm for 3sec, then spreading the resist at 750rpm for 3sec and finally thinning the resist by spinning at 3000rpm for 30sec.

17. Bake in an oven at 120°C for 30 minutes or hotplate at 140°C for 2min.

18. Diesaw 35mmX35mm samples using a 200μm at a blade speed of 7.

19. Solvent clean wafers by washing in acetone for 1min, isopropanol for 1min, methanol for 1min, and DI water for 1min while making sure that the solvents do not evaporate between wash steps.

20. Dehydrate wafer at 200°C for 2min.

11.1.3 Carbon nanotube/fibers

11.1.3.1 Catalyst Patterning

21. Spin on Microchem 4% 950K PMMA in Anisole resist on samples by first dispensing resist on static wafers and then spinning wafers at 4000rpm with a ramp rate of 1000rpm/sec for 60sec.

22. Bake on a hotplate at 185°C for 2 minutes.

23. Expose 100-200nm lines of squares with a 100-300nm pitch using an 30keV accelerating voltage with a 20μm aperture. Use the following parameters for the exposure, given a 100μm square field size use an area dose of 390μC/cm^2 and a 10nm step size.

24. Develop samples in a solution of 2:1 IPA:MIBK for 115sec at 20°C followed by an immediate IPA rinse for 30sec, a DI water rinse for 60sec, and finally spin or N_2 blow dried.

25. Ebeam deposit 10-30nm Ni catalyst at a chamber pressure of <1e-6Torr at a rate of 1Å/sec. Note: Care is taken to minimize time between developing of sample and introduction in to vacuum.

26. Liftoff excess Ni in NMP at 80-90°C for 10-15min, followed by a 5sec sonication.

27. Solvent clean samples by washing in acetone for 1min, isopropanol for 1min, methanol for 1min, and DI water for 1min while making sure that the solvents do not evaporate between wash steps.

11.1.3.2 Growth

28. Grow CNs from catalyst. The following conditions gave the best growth. Chamber vacuum should be less than 0.145 mbar to start, start the flow of 200 sccm NH_3 and increase the temperature to 750°C at a rate of 300°C/min. Once the temperature reaches above 650°C as indicated by the infrared thermocouple, increase temperature to 825°C at a rate of 300°C/min, and spark plasma at 600V and tune system for a plasma power of 150W DC. After 30 sec, increase the flow of NH_3 to 400 sccm and turn on a 100 sccm flow of C_2H_2. After a 30 min growth, turn off the plasma, heater, and both gases, and force cool the chamber with a 2000 sccm flow of Ar while maintaining a chamber pressure of 90 mbar. Samples are safe to be removed when chamber temperatures fall below 200°C

11.1.4 Contacts

11.1.4.1 Deposit Materials

29. Deposit conformal oxide layer, the exact specifications will vary based on pattern but these set of parameters should provide a good starting point. Gases types

and flow rates should be set to N_2O (1420 sccm ±25%), N_2 (1420 sccm ±25%), and SiH_4O (12 sccm ±25%) Platten and showerhead temperatures both should be set to 200°C ±20°C. Last, set the showerhead RF to 380 khz and 100W. This recipe gives an approximate vertical growth of 13Å/s. Grow for 15min.

30. Deposit doped silicon contact material, the exact specifications will vary based on pattern but these set of parameters should provide a good starting point. Gases types and flow rates should be set to SiH_4 (12 sccm ±25%) and 2% PH_3 (20 sccm ±25%) Platten and showerhead temperatures both should be set to 200°C ±10°C. Last, set the showerhead RF to 13.56 Mhz and 20W. This recipe gives an approximate vertical growth of 4Å/s. Grow for 30min.

11.1.4.2 Create Etch Mask

31. Treat wafers with HMDS primer by using a standard vacuum vapor primer oven.

32. Spin on OCG825 resist on wafers by first dispensing resist on wafers spinning at 500rpm for 3sec, then spreading the resist at 750rpm for 3sec and finally thinning the resist by spinning at 4000rpm for 30sec.

33. Bake in an oven at 90°C for 10 minutes.

34. Spin on OCG825 resist on wafers by first dispensing resist on wafers spinning at 500rpm for 3sec, then spreading the resist at 750rpm for 3sec and finally thinning the resist by spinning at 4000rpm for 30sec.

35. Bake in an oven at 90°C for 30 minutes.

36. Expose contacts using a contact aligner with a chrome photomask in hard contact. Expose with a 365-405nm 10mw/cm^2/sec light source for 8sec.

37. Develop in OCG 934 1:1 for 180sec by placing wafer in developer and then agitating the developer. Follow developing with a DI water rinse for 1min and N_2 blow dry.

38. Ash wafers in an oxygen plasma at 1kw for about 15-30min depending on height of carbon nanotubes and thickess of resist.

39. ECR/RIE doped silicon using SF_6(100sccm) at 70mtorr at an ECR=400W/RF=50W power for 1min. Prior to introducing the sample, preclean the system with a mixture of CF_4(40sccm)/O_2(15sccm)/He(15sccm) at 2.1mtorr at an ECR=300W/RF=50W for 10min followed by the etch used for the doped silicon.

40. Solvent clean samples by washing in acetone for 1min, isopropanol for 1min, methanol for 1min, and DI water for 1min while making sure that the solvents do not evporate between wash steps.

41. Ash wafers in an oxygen plasma at 1kw for about 60min to remove all residual resist.

11.1.5 Release

42. Etch the sample in Transene Buffer HF Improved for 1min.

43. While sample is still wet place in 3 exchanges of DI water, a solution of 50% ethanol in water, a solution of 70% ethanol in water, a solution of 90% ethanol in water, and finally 2 exchanges of 100% ethanol at 4 minutes for each step and taking that the sample remains wet between each step.

44. Again, while sample is still wet place in a critical point dryer filled with 100% ethanol. Critical point dry sample using a purge time of 10min.

11.1.6 Optional: Bond Pads

42. Treat wafers with HMDS primer by using a standard vacuum vapor primer oven.

43. Spin on AZ5214E resist on sample by first dispensing resist on sample spinning at 500rpm for 3sec, then spreading the resist at 750rpm for 3sec and finally thinning the resist by spinning at 1500rpm for 30sec.

44. Bake in an oven at 90°C for 30 minutes.

45. Expose bond pads using a contact aligner with a chrome photomask in soft contact. Expose with a 365-405nm 10mw/cm^2/sec sec light source for 2.5sec.

46. Bake in an oven at 90°C for 30 minutes.

47. Flood expose sample using 365-405nm 10mw/cm^2/sec light source for 45sec.

48. Develop in AZ 422 for 105sec by placing wafer in developer and then agitating the developer. Follow developing with a DI water rinse for 1min and N_2 blow dry.

49. Ebeam deposit sample/10nm Ti/100nm Au. Start with a vacuum pressure <1e-6Torr. Deposit Ti at a rate of 1Å/s. Deposit Au at a rate of 3Å/s.

50. Lift off sample by placing in acetone until excess metal has been removed, typically >1hr. Ultrasonicate sample for 1min in acetone.

51. Solvent clean samples by washing in acetone for 1min, isopropanol for 1min, methanol for 1min, and DI water for 1min while making sure that the solvents do not evporate between wash steps.

52. Proceed with Release.

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